EUVL for HVM: Progress Update

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Intel Corporation

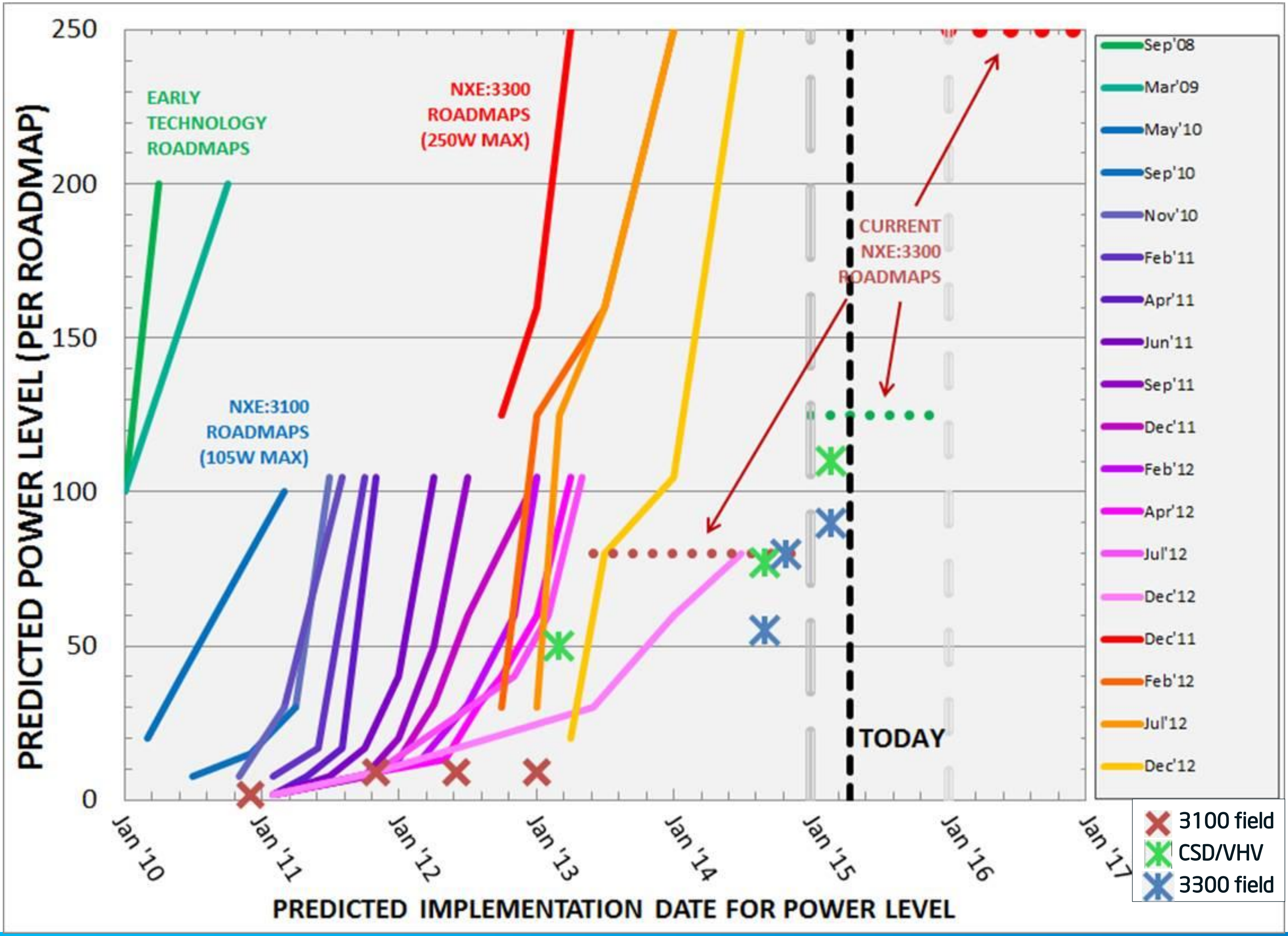
Outline

- EUV source and system performance
- EUV/193i complementary patterning
- EUV infrastructure

What about exposure tool performance gates committing a process node to EUV?

- Technology Development requires rapid information turns
  - Availability: tool must be up to run TD wafers without delay
- HVM requires reasonable COO and predictability, driven by:
  - Productivity (mostly source power)
  - Availability (mostly source availability)
  - OpEx (mostly source consumables)

Two years of solid progress on source power



As of PMJ in April

Worldwide fleet 40-80W

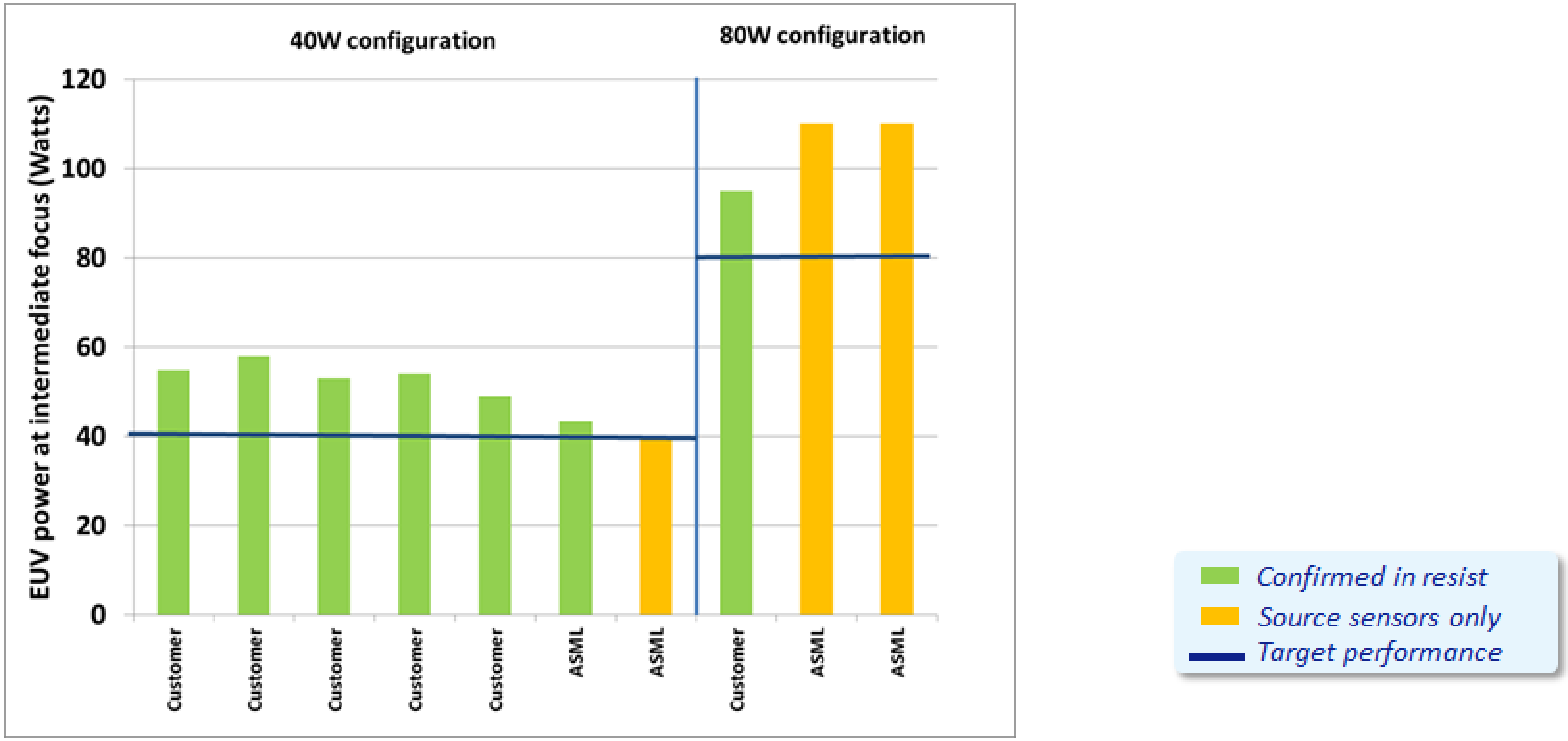
Multiple systems capable of >90W

All systems demonstrated capability to meet performance target

ASML

public

Slide 1



All results normalized to clean collector conditions

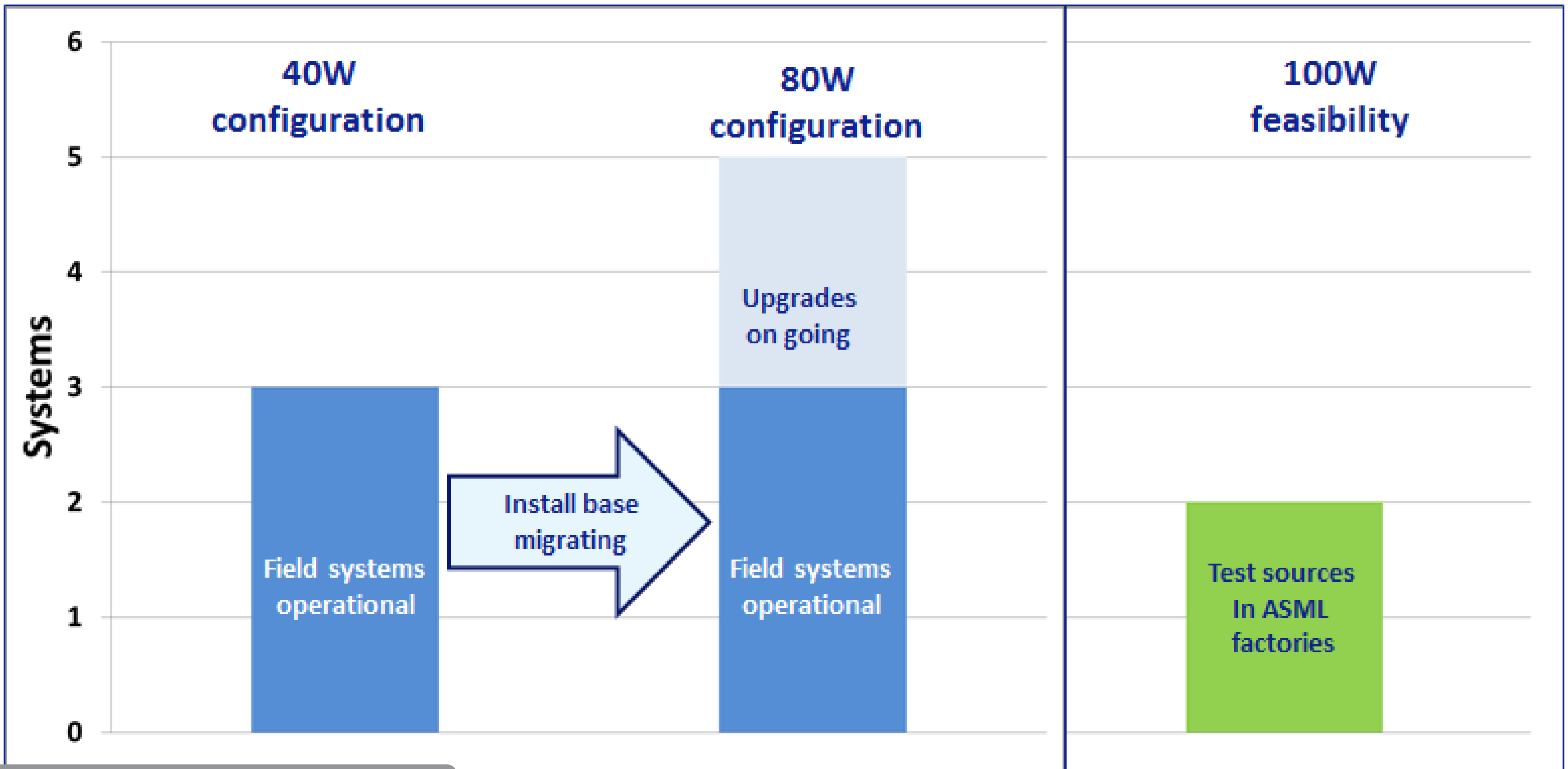
Slide courtesy ASML

Install base quickly migrating to 80W config

NXE:3300B install base migrating from 40W to 80W configuration

Upgrade enables 2x improvement in power, ~10% availability gain

Public



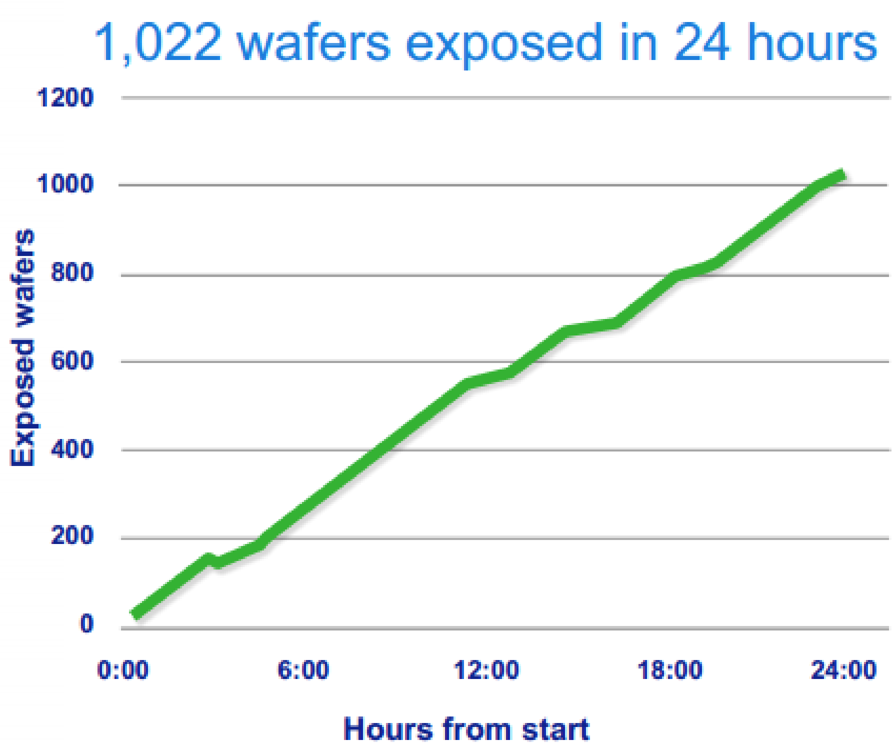
Slide courtesy ASML.

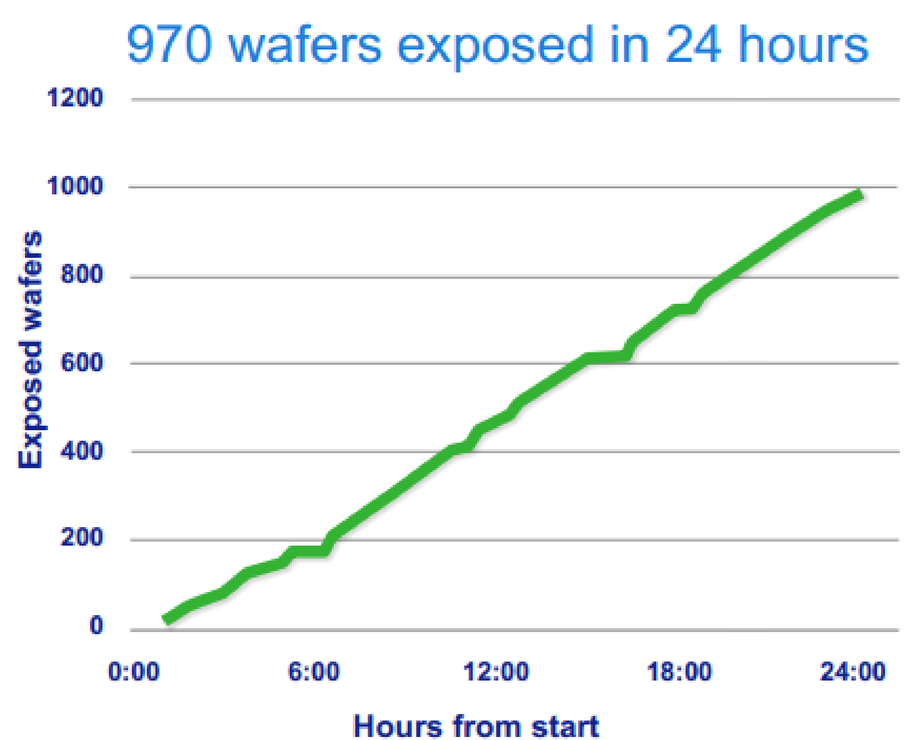
Short-term productivity >1000wpd

Today: 1,000 wafers per day capability demonstrated

On a field system, using customer exposure conditions, on 2 different days

ASML
Public
Slide 5
February 2015

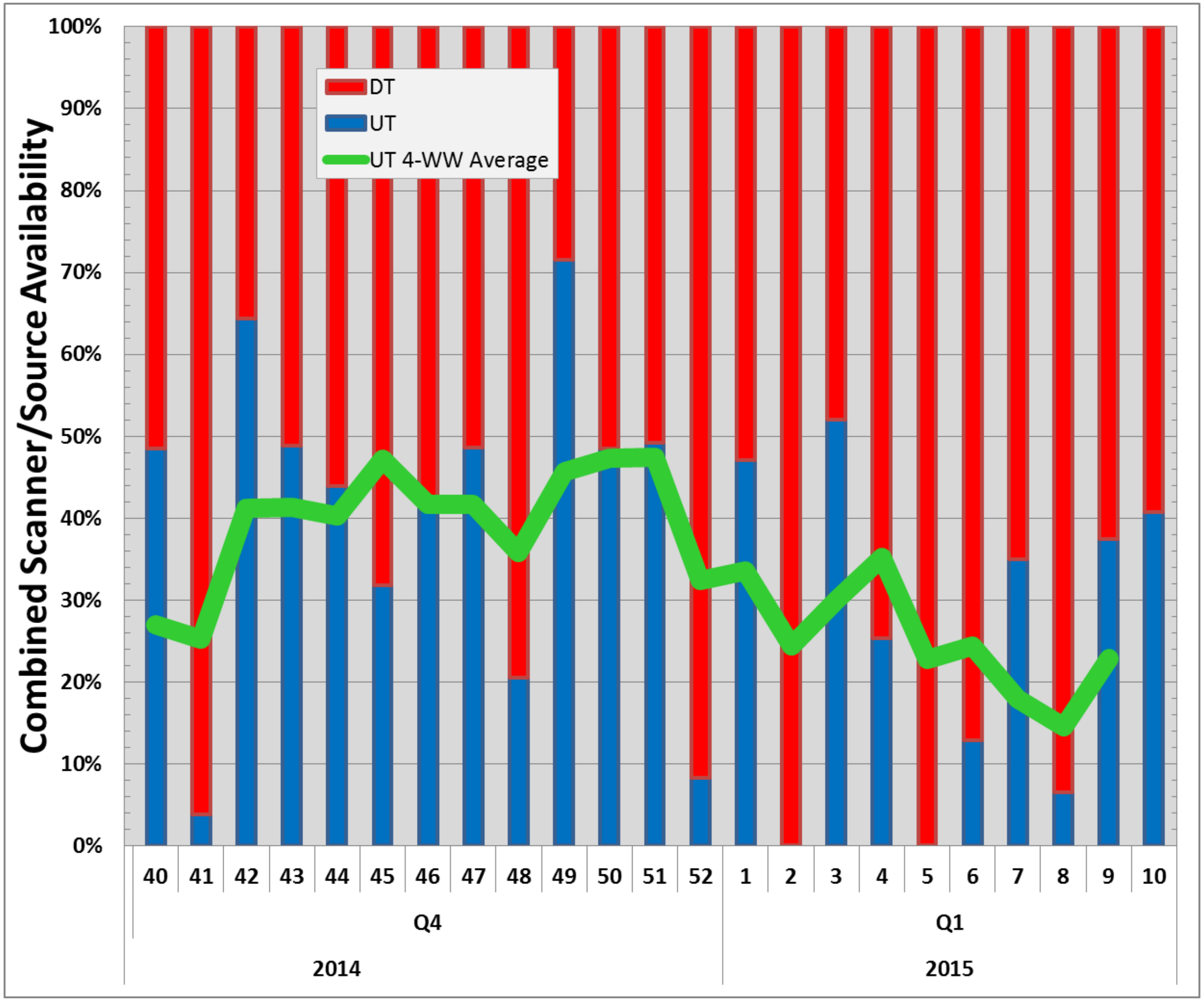




80W source configuration

Alberto Pirati, SPIE Advanced Lithography, 2015

However…



Availability and predictability are still poor

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Extended demo of availability and predictability

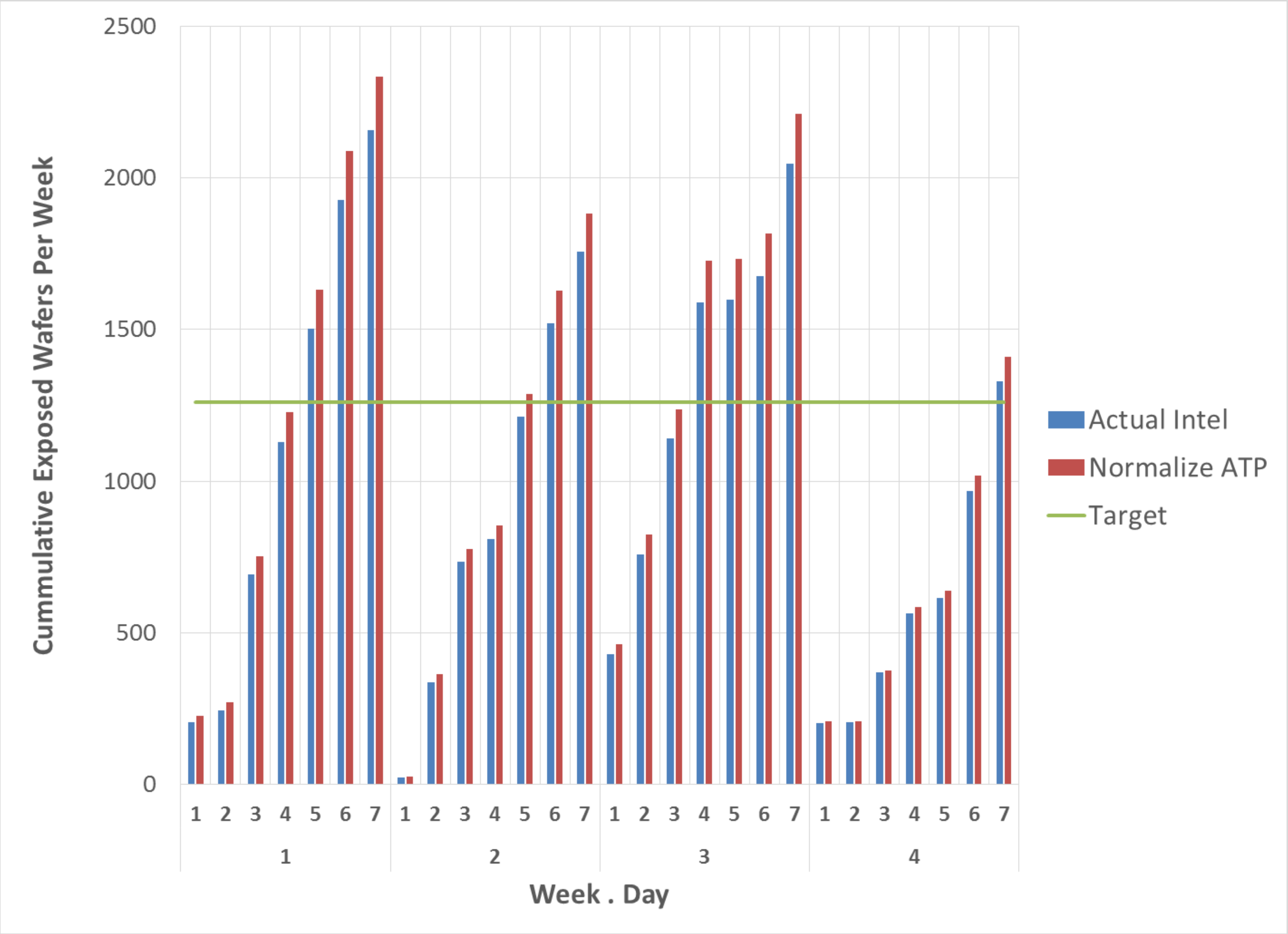
- 21hrs/day wafer cycling with mix of test-chip wafers (CDs, overlay, in-line defects, e-test) and bare silicon
- 3-hr daily Intel engineering window (no tool work)
- Availability counted 24hrs/day. Wafer output targets set for 21hrs/day in 40W config.
- Only good wafers (meeting dose control specs) counted
- Goal: demonstrate tool can run as advertised for 40W config today, *including imaging and overlay*

Targets and results from 4-week demo

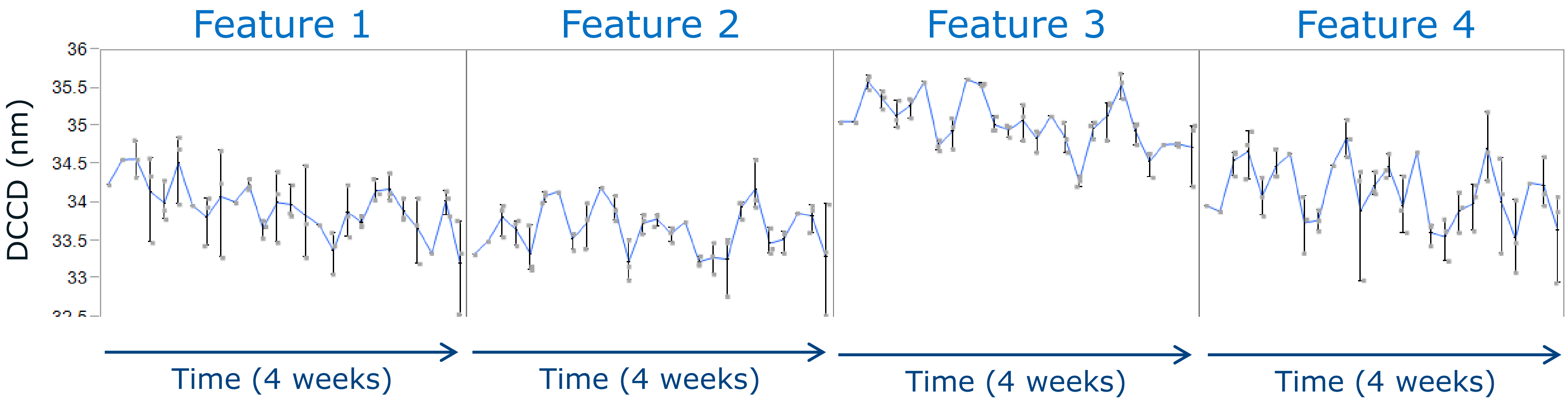
	Nominal Target	Demo-Time Adjusted Target	Result
Availability (scanner + source)	**46%**	**46%**	**61%**
TPT - good wafers per day	**180**	**170**	• **280** normalized WPD • ***260*** actual exposed WPD (raw count)
TPT - good wafers per week	**1260**	**1189**	• **1959** normalized WPW • ***1822*** actual exposed WPW (raw count)
No consecutive DT > 72hrs	**<72hrs**	**<72hrs**	Max consecutive downtime = **36hrs** (DG swap + Sn catch drain + RF generator failure/replacement on PA0)

- Goal: demonstrate tool can run as advertised for 40W config today
- Targets based on 125 fields/wafer at 15mJ/cm^2 dose
- Actual wafers exposed were a variety of shot maps and doses, so "normalized" count converts to equivalent at 125 fields/15mJ
- Integrated test-chip wafers allowed verification of imaging, overay, and defects throughout demo → results all good

Demo cumulative wafers per week

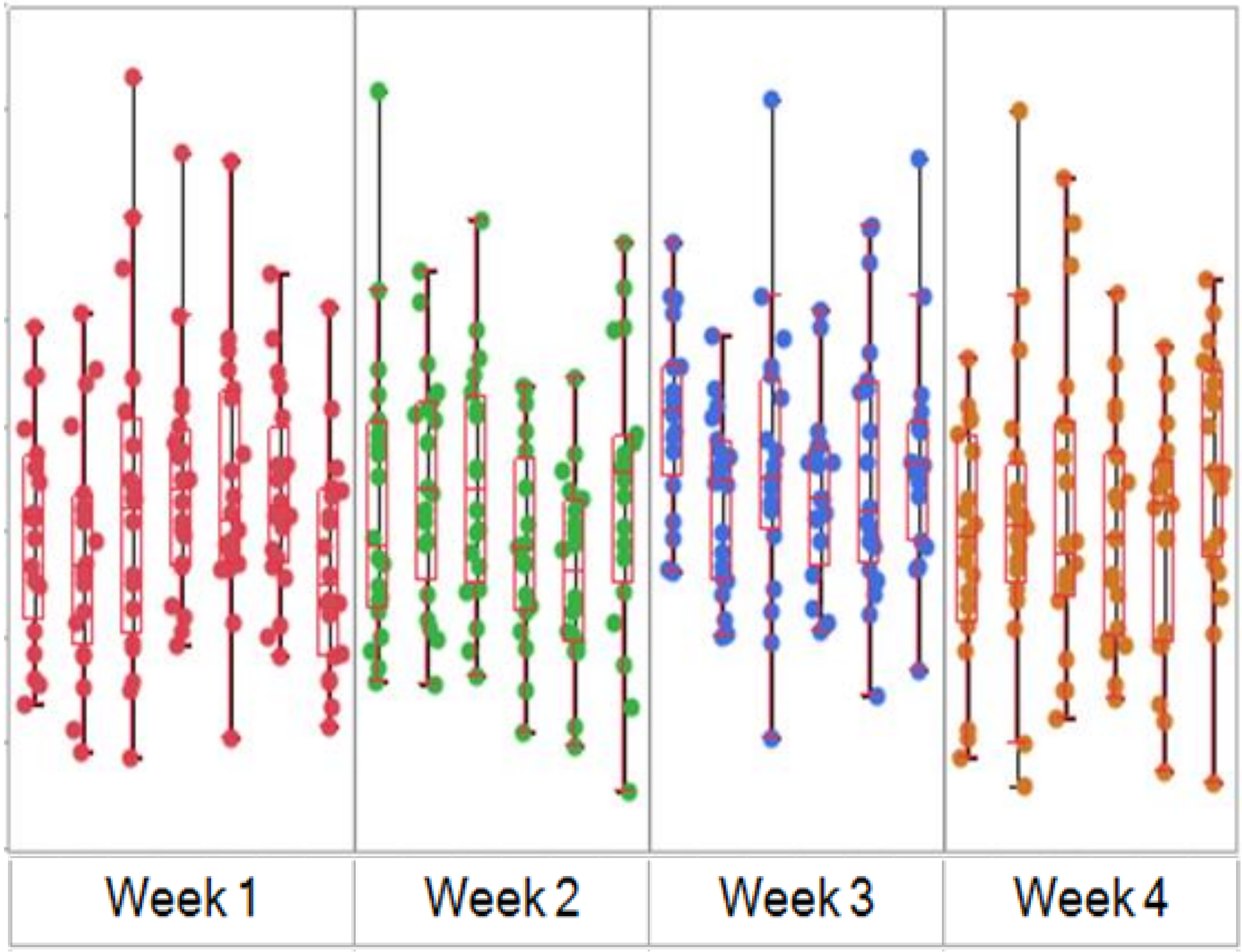


Demo hole CD trend



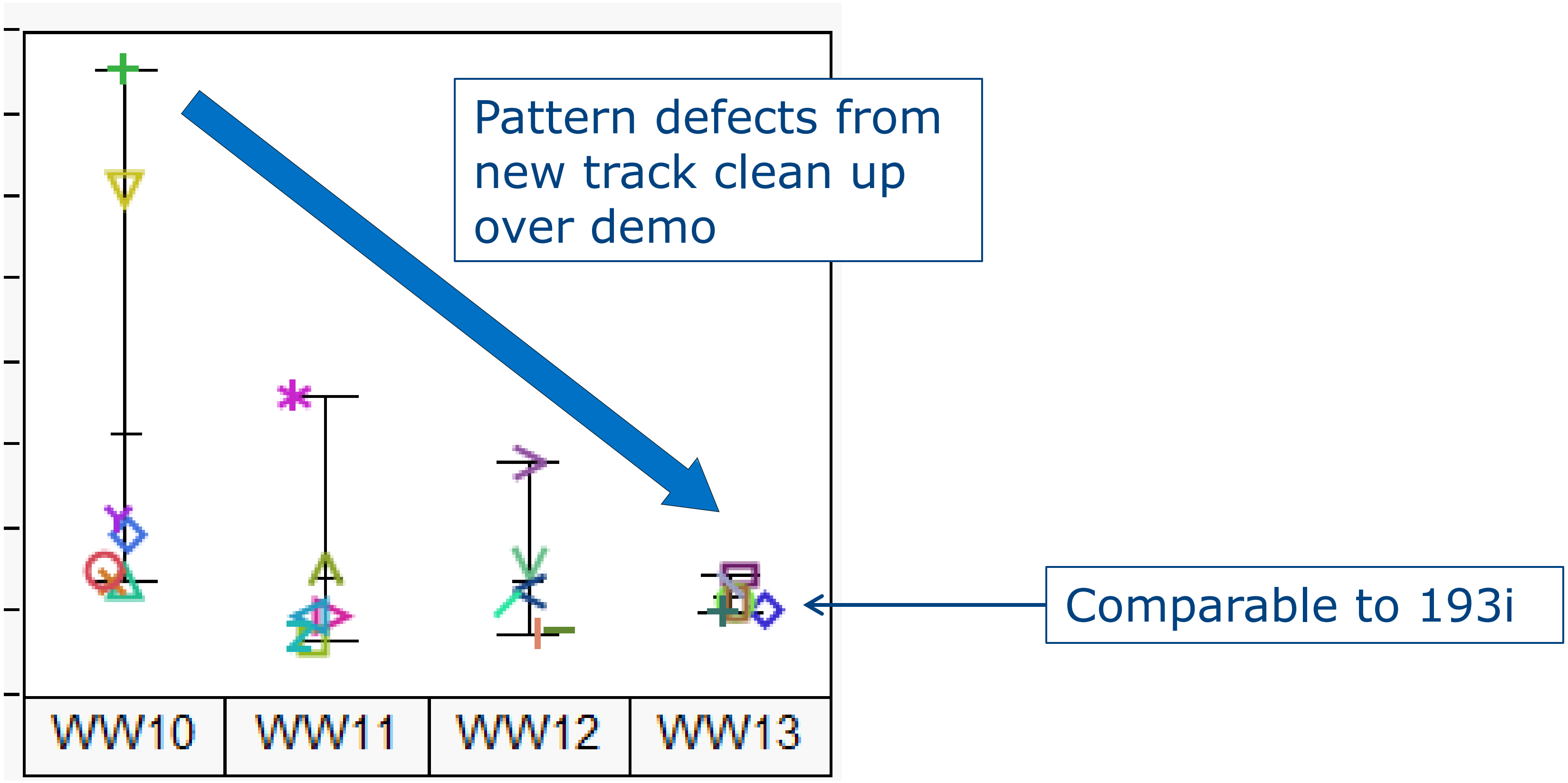
- OK. Some trends. No APC applied

Demo e-test trend



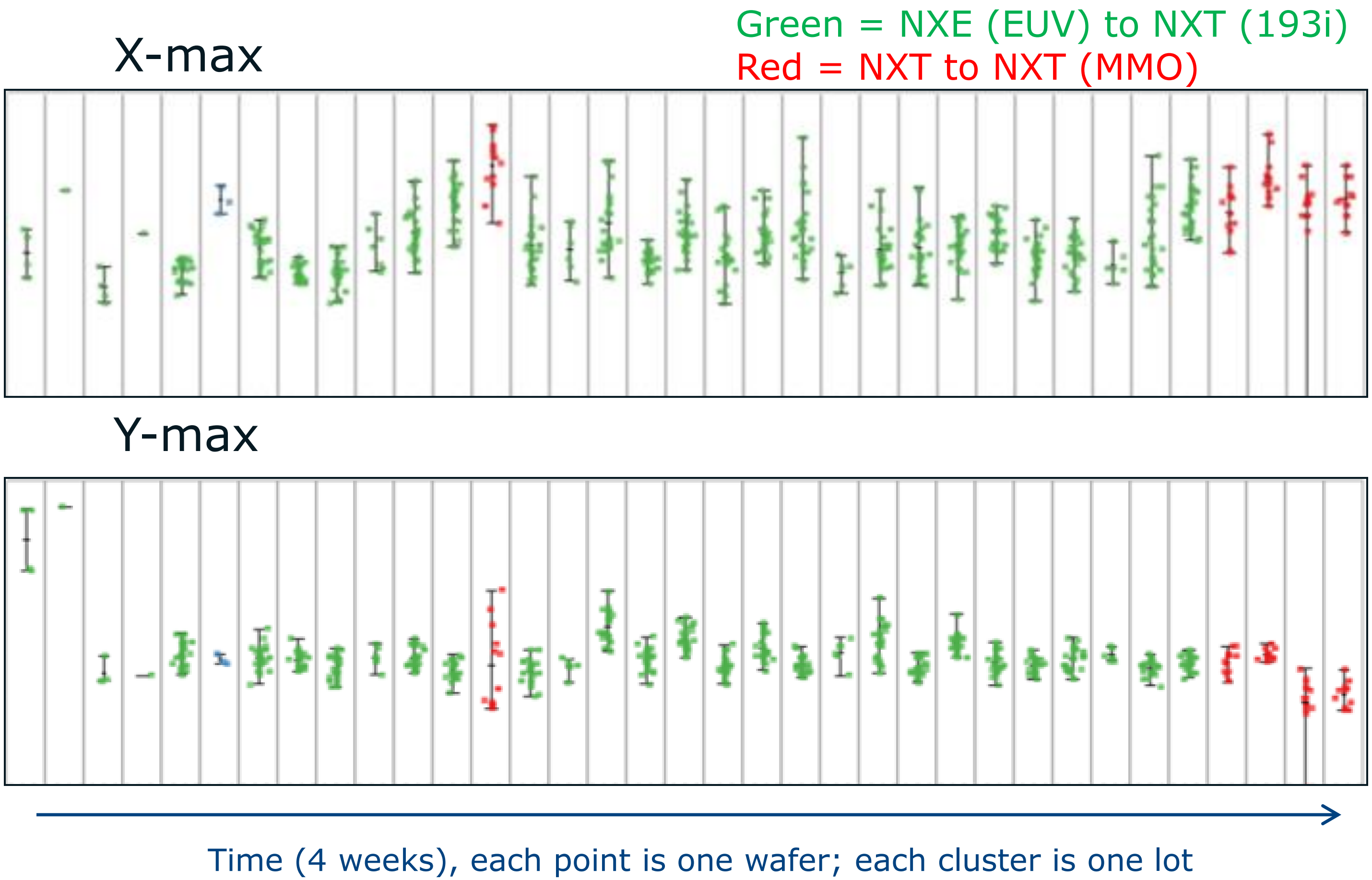
- Stable.

Demo in-line defect trend



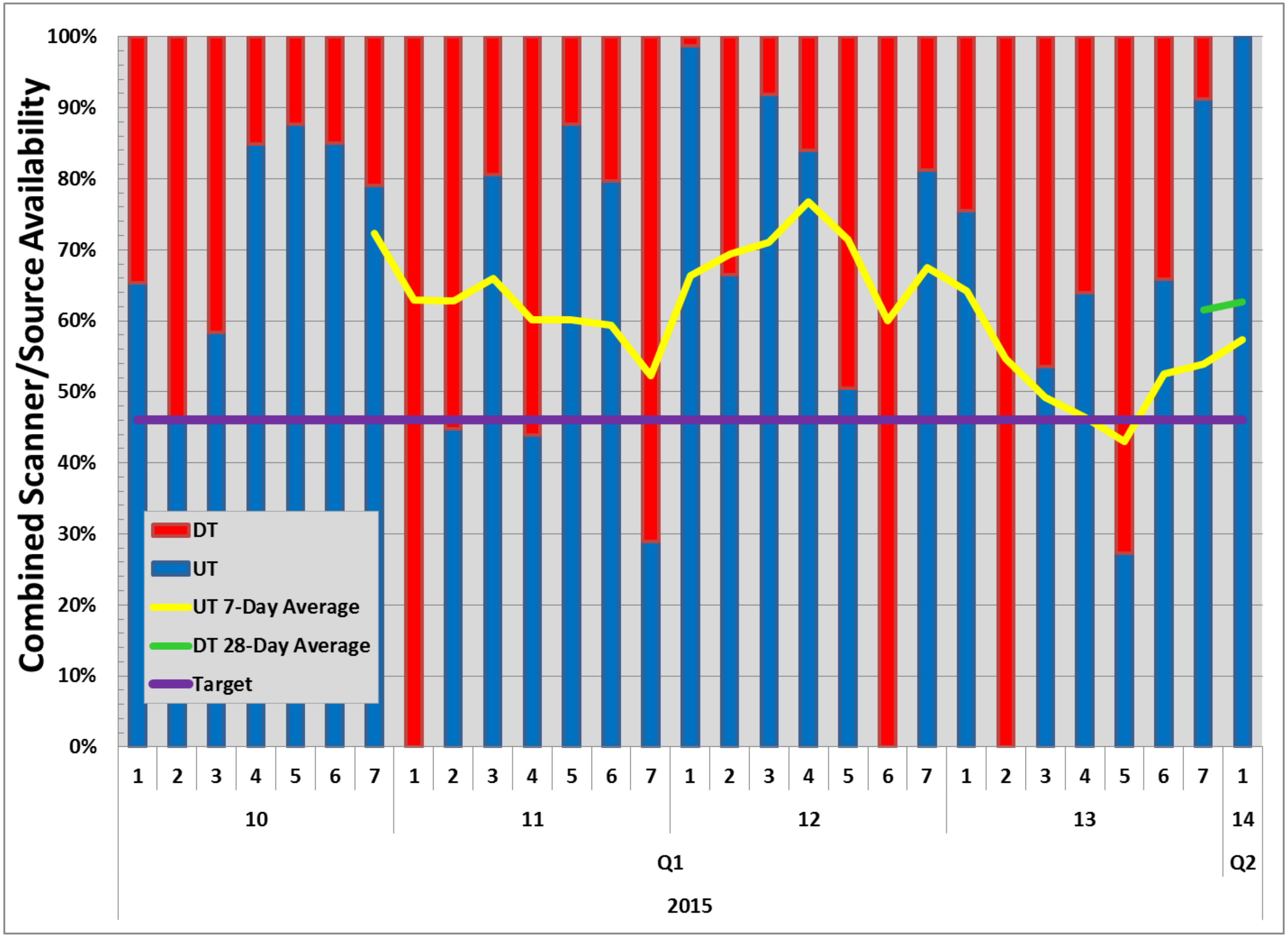
- Track cleans up over time. Scanner contribution is OK.

Demo overlay trend



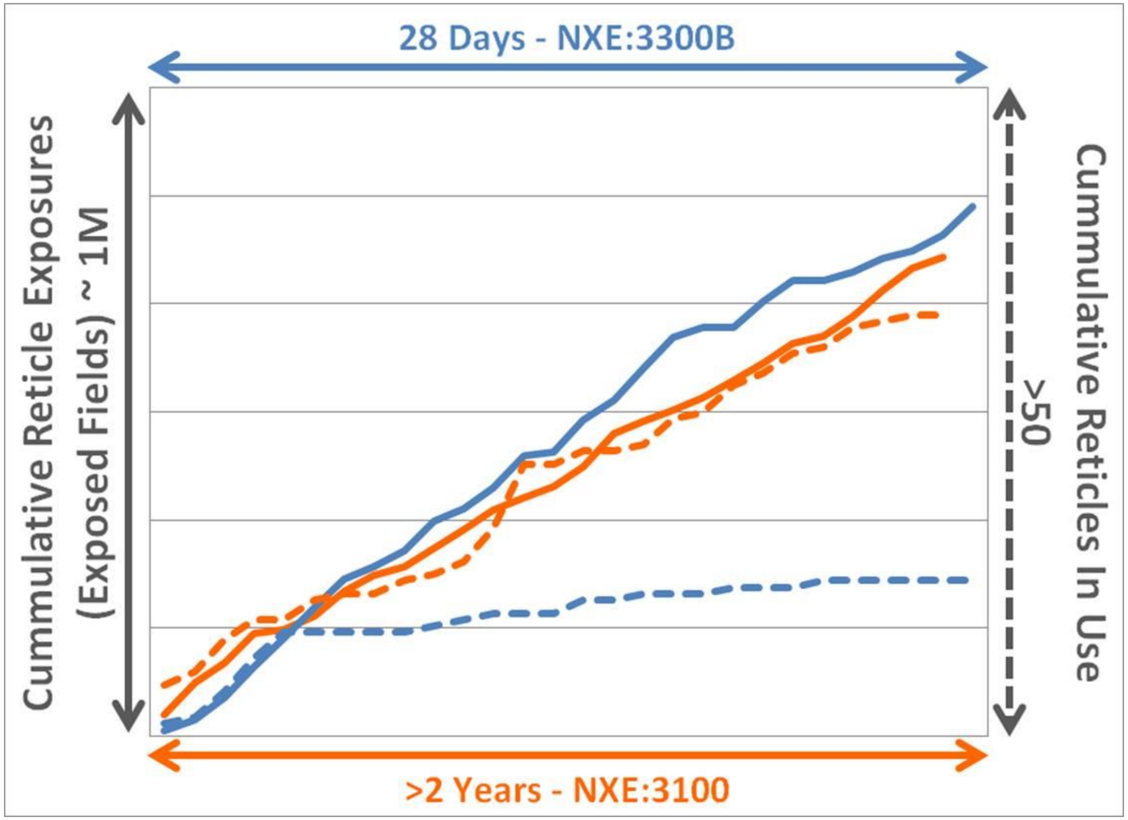
- OK. No overlay penalty for EUV-193i versus 193i-193i MMO.

Demo availability (4 weeks)



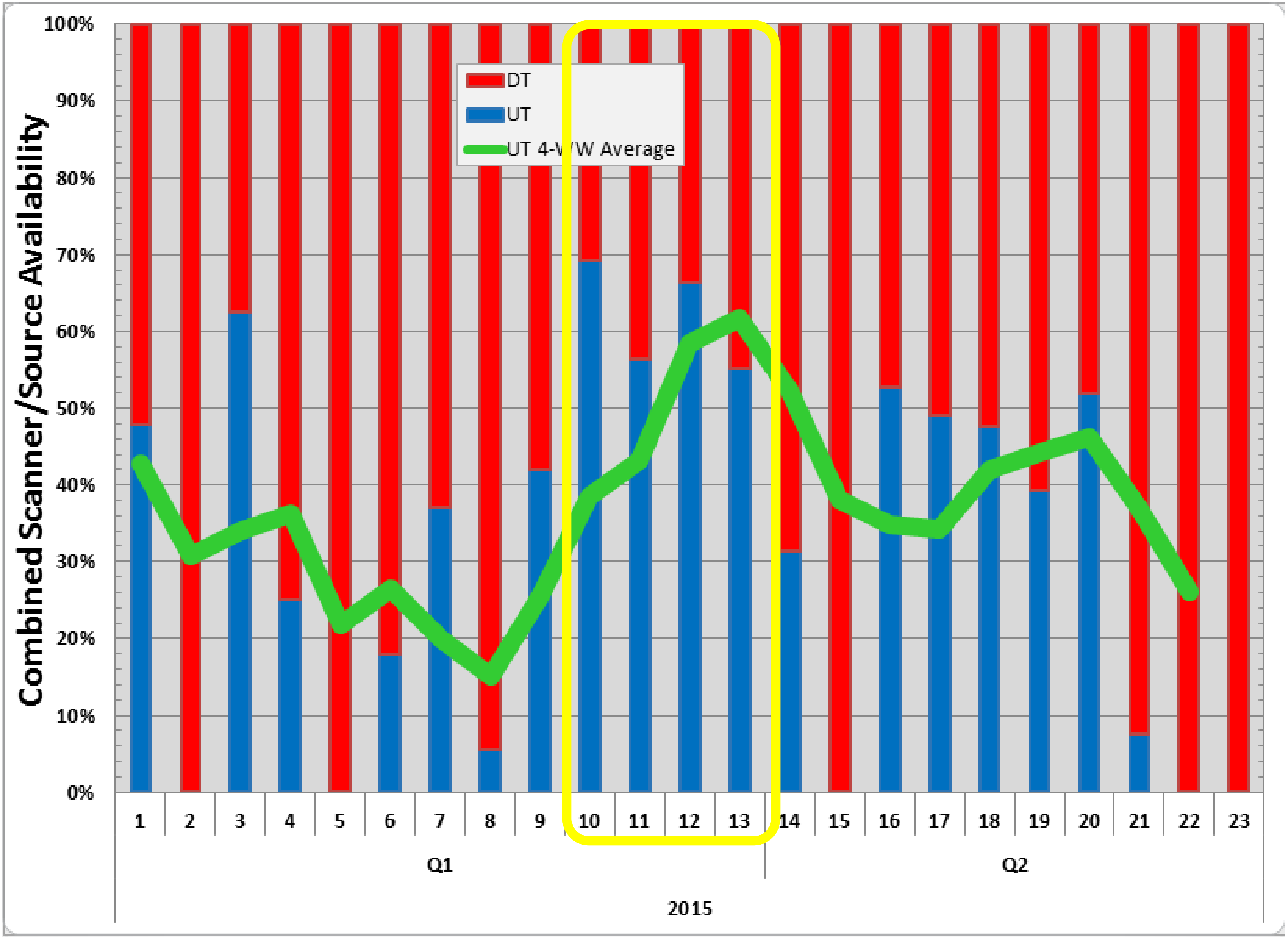
- Far from OK for production, but better than expected for current 40W config

NXE:3300 accelerating learning on EUV reticle usage



- > 300 reticles associated to NXE scanner platform fabricated since 2010
- The NXE reticles are closely monitored in their functionality, reliability and utilization.
- Several plates, each utilized over 2 years, exposed to >10kJ EUV irradiation
- NXE:3300B now allows study with higher-power and throughput
- Only experience with pellicles in place was demonstration with full-size proto pellicle

Over longer term, availability is unstable



Summary of EUVL status

- Two years of solid progress on EUVL
  - Eight 0.33NA systems shipped, generally meeting all performance specs not related to source power
  - 80W config proliferating quickly, and 100W (@IF) MOPA/PP demonstrated in the field
  - ~500wpd, then ~1000wpd in short-term (1-2 day) demonstrations
  - 4 week demonstration of availability and output consistent with 40W tool configuration, and stable imaging and overlay performance

- Introduction in production is a question of “when” rather than “if”
  - Availability, stability and operating cost are still concerns
  - Need to ensure infrastructure does not gate HVM

Outline

- EUV source and system performance
- EUV/193i complementary patterning
- EUV infrastructure

How will EUV be used at introduction?

Intel Lithography Roadmap
Circa 2002

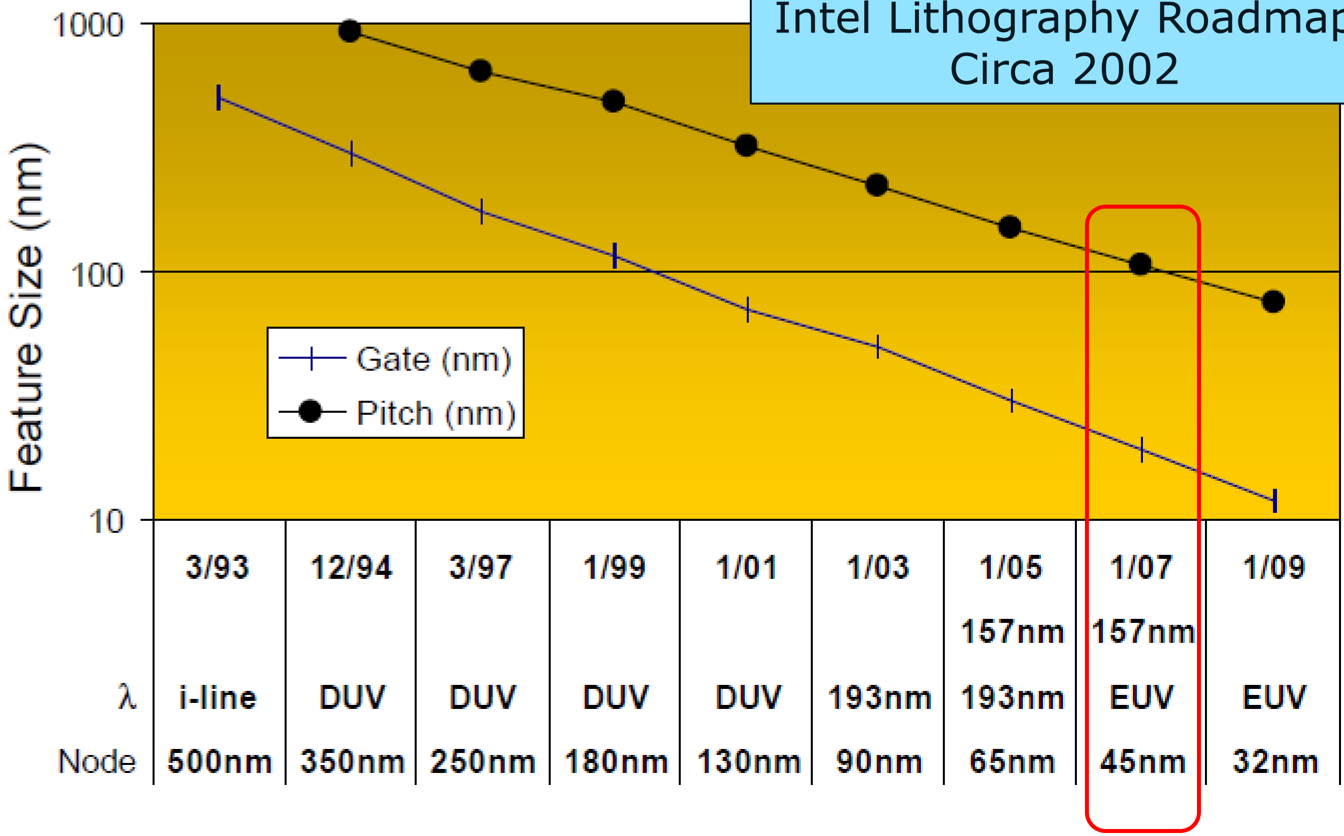
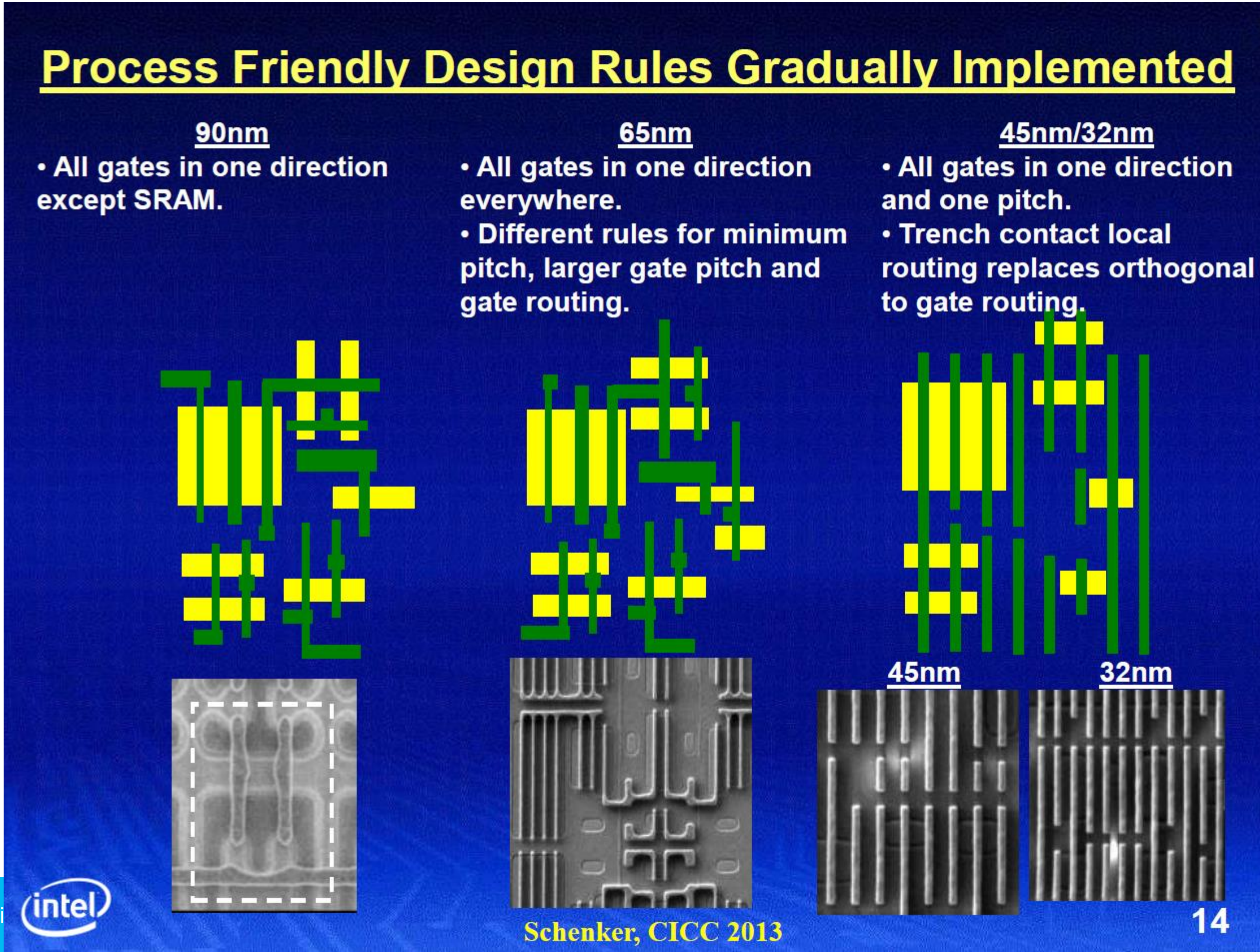


Figure 1: Intel Lithography Roadmap

Plan A: Insertion as high-k1 single exposure

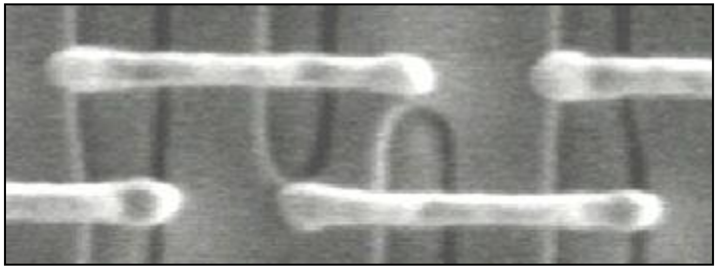
OK, so what is Plan B?

A lot has happened in 13 years…

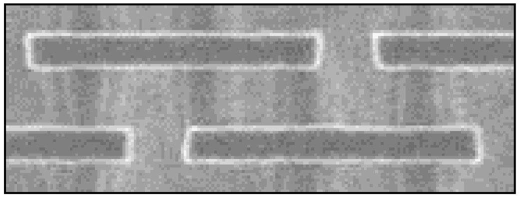


Restricted DR & grating/cut are here to stay

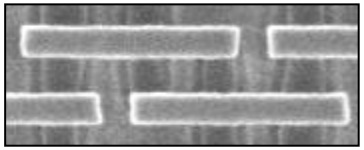
SRAM cell scaling



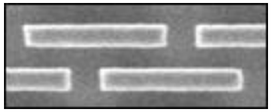
65 nm, 0.570 um^2



45 nm, 0.346 um^2



32 nm, 0.171 um^2



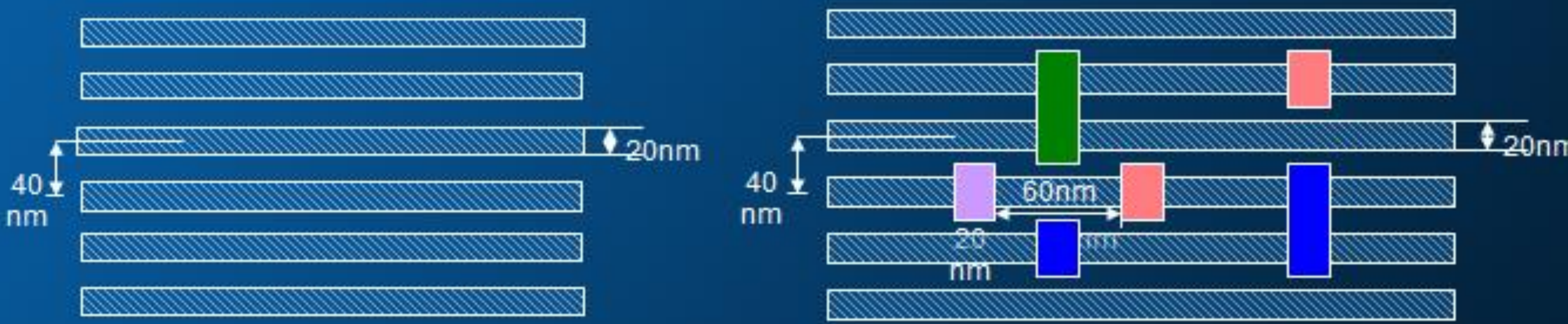
22 nm, 0.092 um^2

grating+cut litho

- Gradual introduction of stricter DRs was density-neutral or better
- Improved control of features beneficial to device performance and yield
- These layouts are here to stay, regardless of the exposure wavelength
- Only question is optimal techniques for doing gratings and cuts

“Complementary” patterning proposed by Yan Borodovsky ~2010

ArF Only Patterning



1 193i w/PD to form gratings + 4 193i Masks/Exposures to form Pattern = 5 Mask
5 Exposures

Complementary Patterning

CDU, LWR <2nm 3s

CDU, LWR <4nm 3s

1 Mask/1 193i Expose + 1 Mask/1 EUV Expose or 0 Mask/1 EBDW Expose

1 193i w/PD to form gratings + 1 EUV Masks/Exposure or 0 Mask/1 EBDW Exposure

Total 2 Masks/2 Exposures or 1 Mask/2 Exposures

Yan Borodovsky, KLA-Tencor LUF, Feb.21st 2010, San Jose , Ca, USA

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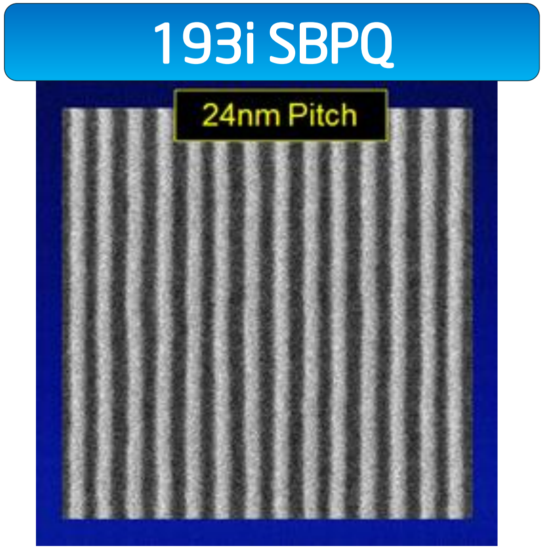
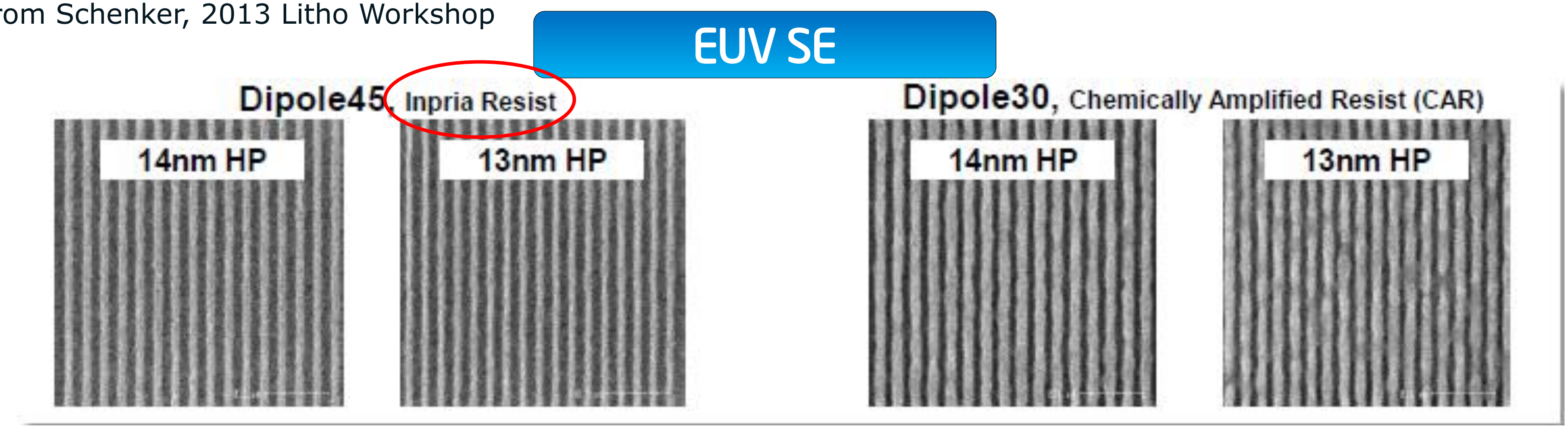
Optimal choice for grating



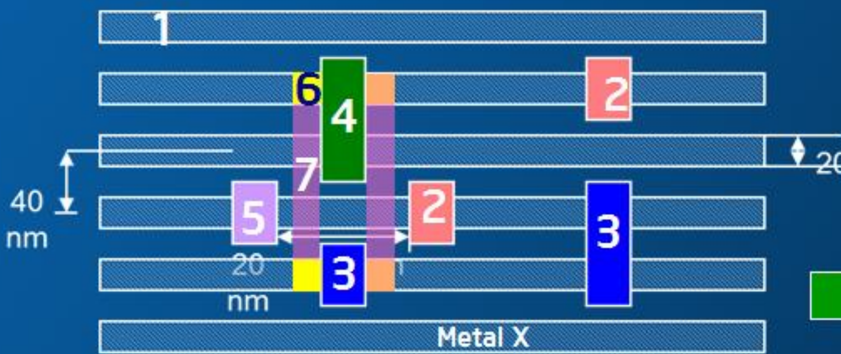
From Schenker, 2013 Litho Workshop

- Today, 193i + SBPQ is the better option for grating (~1/3 cheaper than EUV)
- In long term, need to quantify full EPE budget for each option (LER, MMO, "pitch walking", spacer variability) and reconsider for mature EUV power and CoO

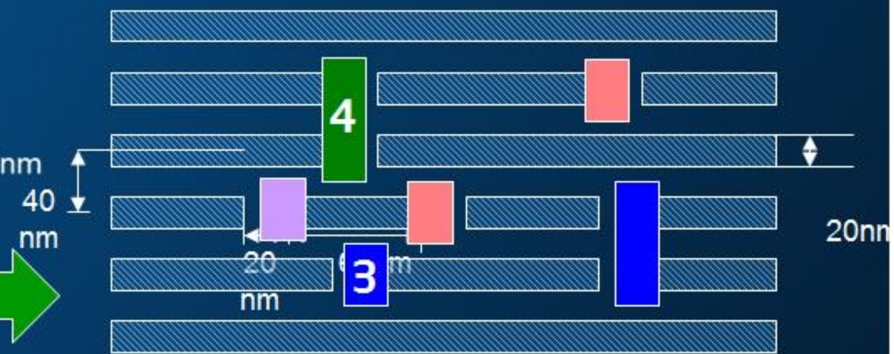


From Brandt *et al.*, EUVL Symposium, 2013

Cut/Via/Metal Non-Scaling Overlay is ultimate limit to amount of Cut and Via split masks

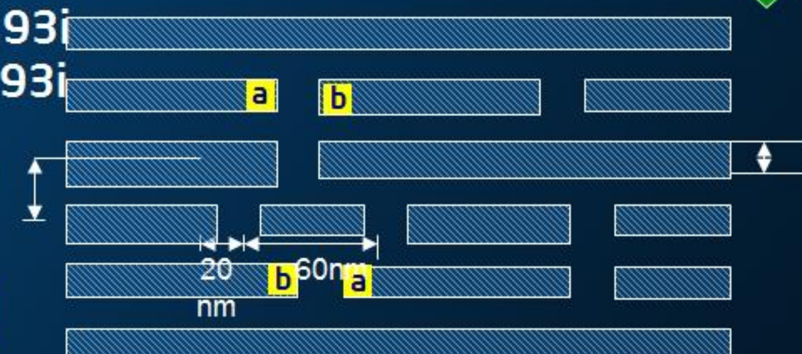


Design: #2-#5 Cuts, #6 Vias, #7 Mx+1

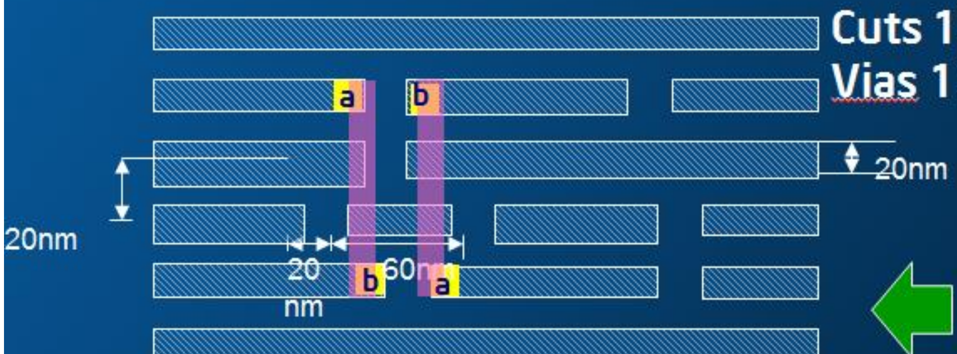


Cuts Printed with some OL errors

Cuts 193i
Vias 193i



Vias "a" aligned to Cut Mask #3&#4
Vias "b" aligned to Cut mask #3&#4



Whichever Via mask one aligns
Metal x+1 to there is a problem

This is Ultimate limit to Over-scaling with Pitch Division

Y.Borodovsky, Alternative Lithographic Technologies VII, Conference 9423, 23 February 2015, San Jose, CA, USA

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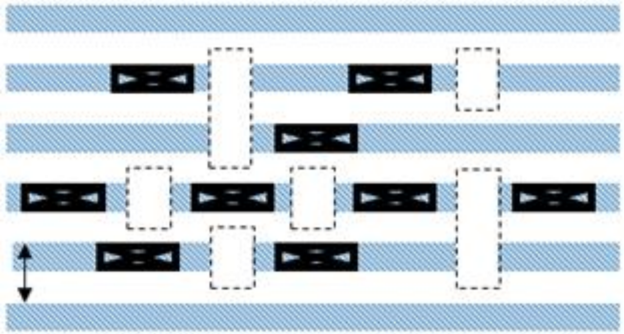
EPE & cost drive Complementary EUV/193i



- EPE budget ultimately limits scaling of layout
- Grating/cut is still optimal for metal layout. Note: only one tight alignment in each direction.
- Critical issue for EPE is keeping all cuts on one mask and all vias on one mask. Resolution of EUV allows this with cost parity at ~1:3 EUV:193i
- 193i + n * SPD can create gating at ~1/3 cost of EUV at 250W

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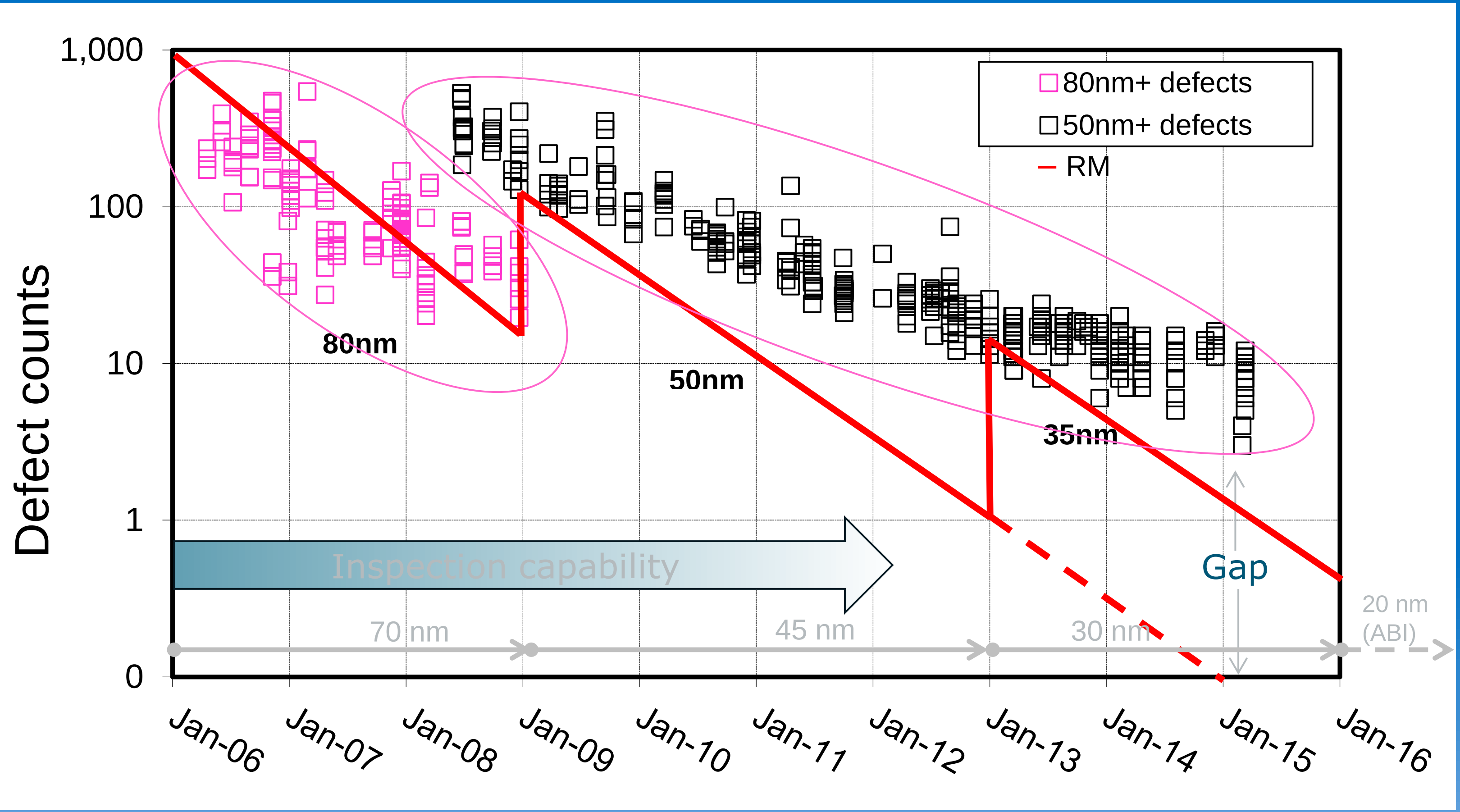
EUV Infrastructure Readiness Snapshot

EUV infrastructure has 8 key programs

2 are ready or near-ready now, 4 are in development, 2 have significant gaps

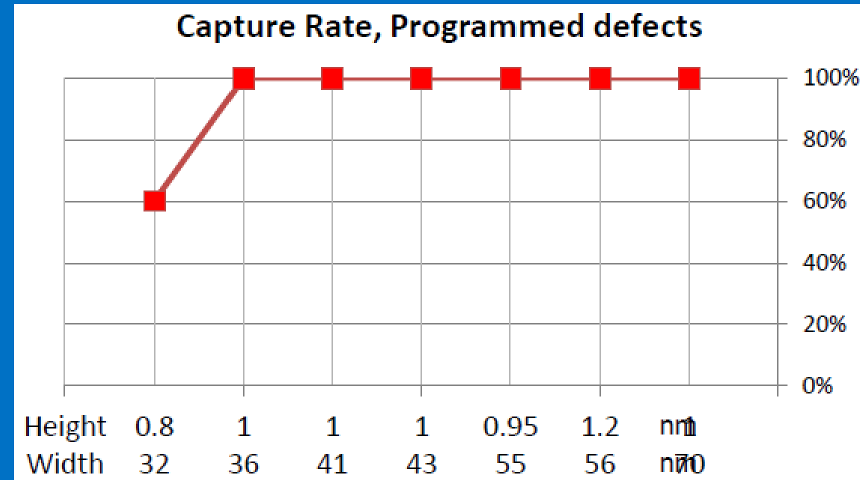
- **E-beam Mask Inspection:** HVM capable tool exists
- **Actinic Blank Inspection (ABI):** EIDEC-led tool development program
- **EUV resist QC:** Industry-wide QC center finalizing definition
- **AIMS Mask Inspection:** SEMATECH-led tool development program
- **EUV blank quality:** Process and yield improvements ongoing
- **Pellicle:** ASML commercializing
- **Blank multi-layer deposition tool:** Improving defect results. Multiple deposition techniques being evaluated to define HVM tool approach.
- **Post-pellicle mask inspection:** APMI not on timeline for insertion. Need other options.

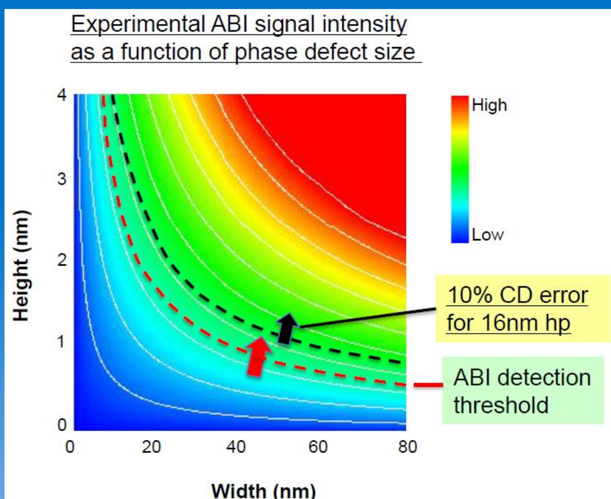
EUV mask blank ML defect trend

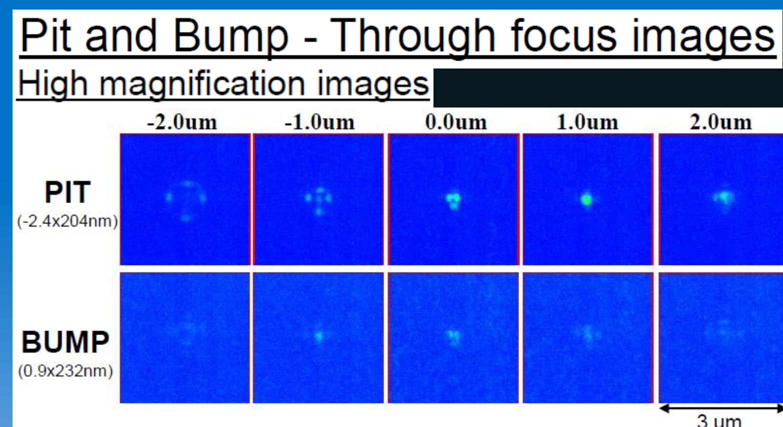


- EUV blanks with single digit (ML) defect count at 50 nm become commercially available
- Gap to the RM still needs to be closed for HVM
- Advanced inspection capability is required for further defect reduction

ABI Tool Development at EIDEC/Lasertec







- LT-ABI HVM prototype is designed to detect 20nm defect with Phase/Amplitude and Pit/Bump classification

- Reported at 2014 EUV Symposium by Lasertec

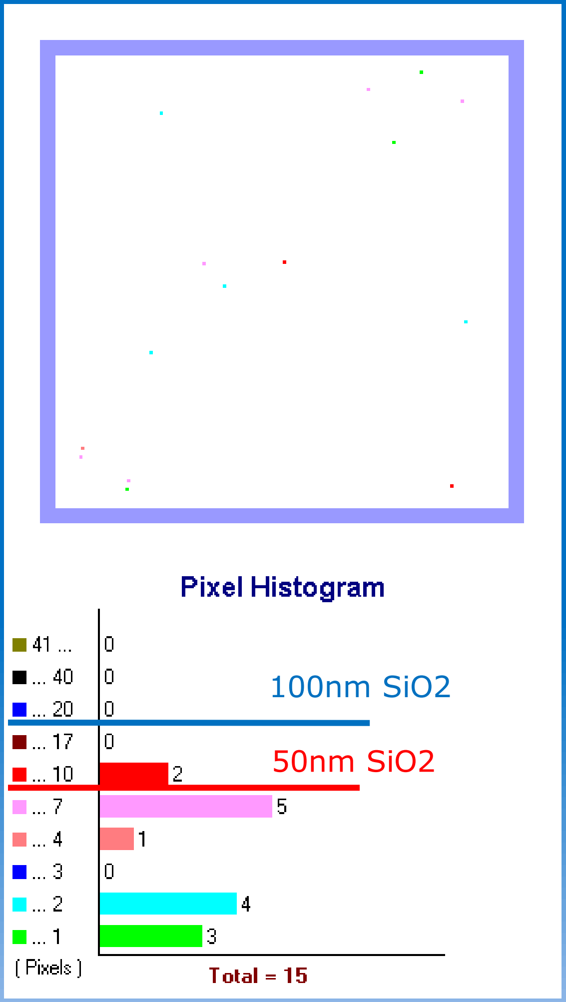
Defect size measurement

Programmed phase defect images from high magnification optics

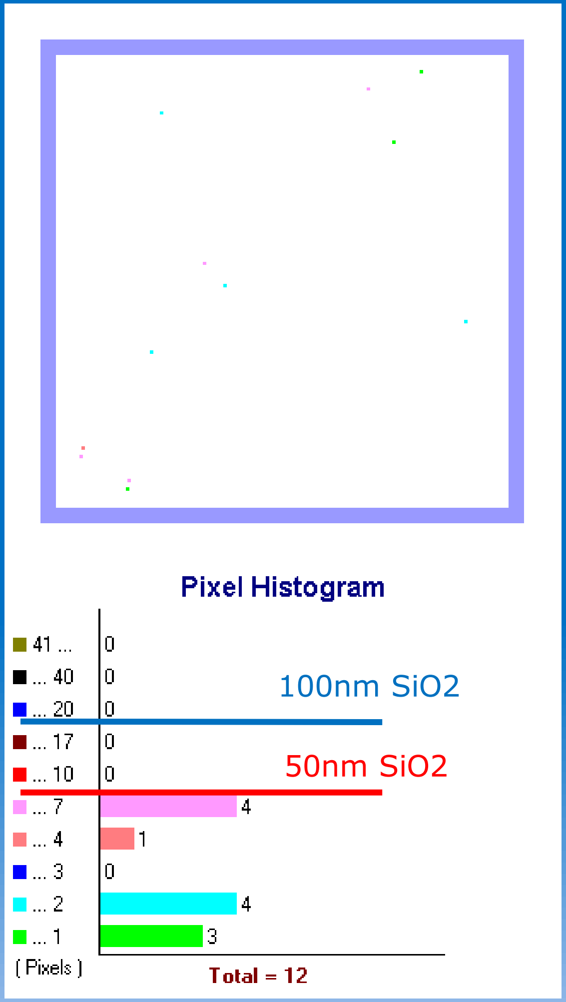
Defect width by AFM	72nm	101nm	108nm	120nm	154nm
Defect images by high Mag. review					
Defect Diameter from ABI images	55nm	76nm	95nm	112nm	120nm

AGC EUV blank ML defect map

Q4/14 ML Blank Total defects



Q4/14 ML Adders



Slide courtesy AGC

Blank defect / mitigation summary

- Blank defect trend at 50nm solidly in single-digit range, making mitigation effective
- ABI in regular use, allowing sampling at 20nm SEVD
- Champion blanks approaching single-digit defects with ABI inspection
- ABI defect location accuracy approaching 10nm target
- Still need engineering work to define blank fiducial strategy compatible with low defects and placement accuracy

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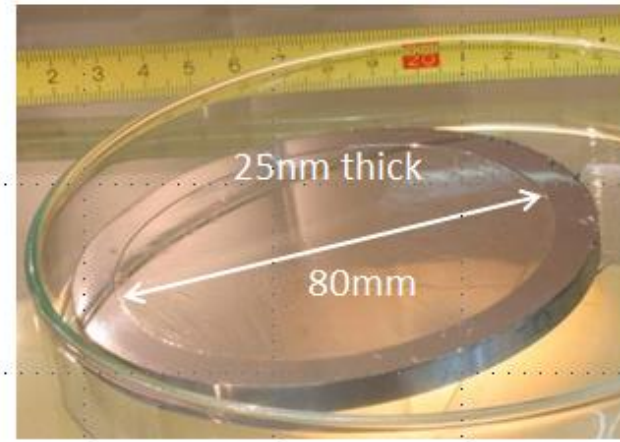
Membranes as of February 2013

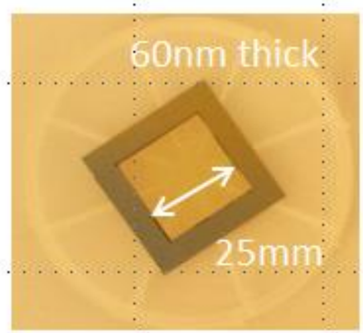
As presented at 2013 ASML Technology Symposium

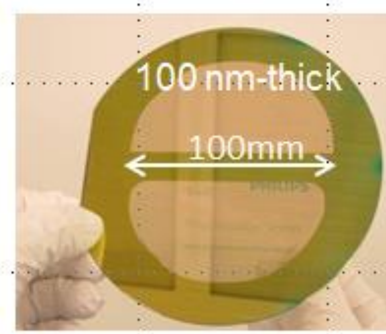
ASML

Free-standing pellicle can be manufactured on large areas

- ASML is investigating several materials, including:
- **Multilattice Pellicle**
  - Si/Mo/Nb-based multilayer
  - Free-standing : no support grid
  - Status
    - 86% EUV transmission
    - 20-25nm thickness
    - 80mm diameter
- **Poly-Silicon Pellicle**
  - Manufactured from standard silicon wafers using standard semiconductor manufacturing process
  - Free-standing : no support grid
  - Status:
    - ~ 80-82% EUV transmission
    - 60nm thickness
    - 25x25mm² area
    - Size up to 100x50mm (100nm thick)







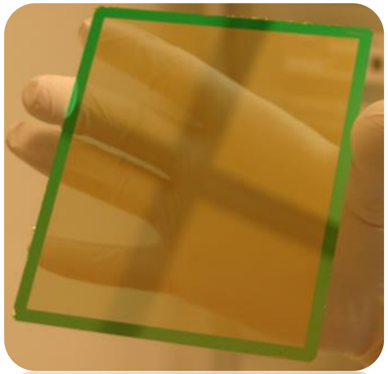
Foil shown in 2013 courtesy ASML

Wafers successfully exposed in NXE:3100 with a full-size prototype pellicle

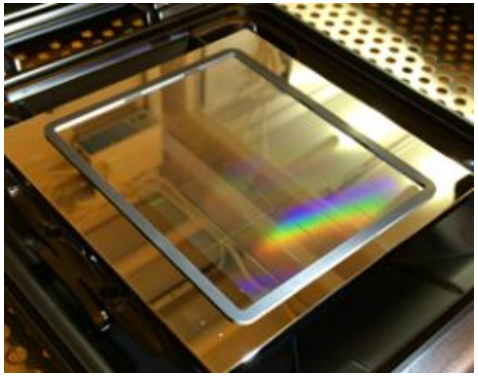
Full size prototype film

Full size prototype frame mounted to reticle

Full size prototype frame and film mounted to reticle



103mm x 122mm (~85% EUV transmission)



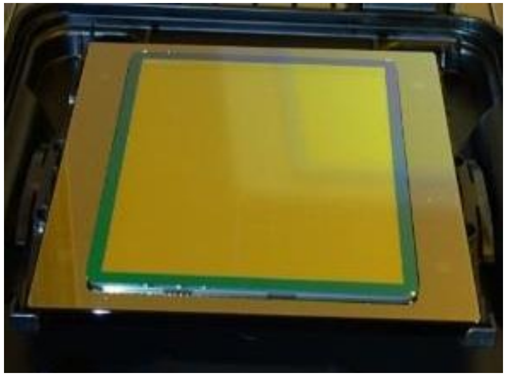
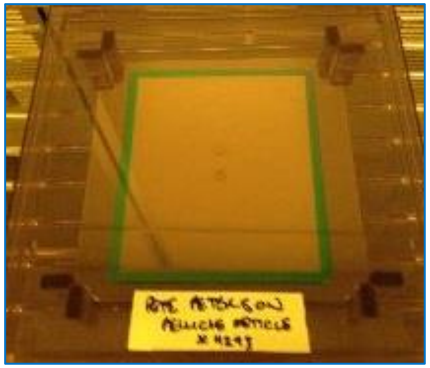


Image and mechanical testing of full size prototype pSi pellicles completed

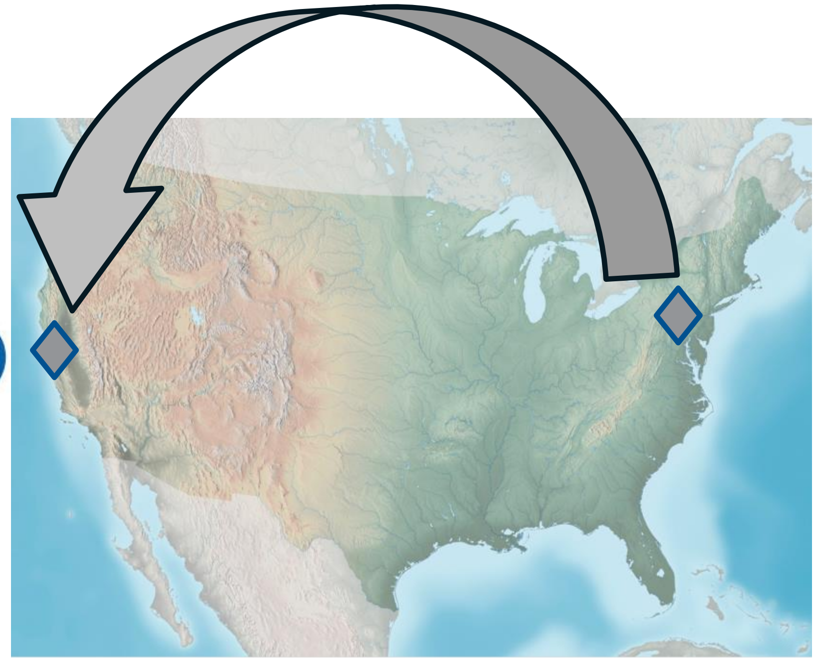
Pictures courtesy ASML, as shown by Sang Lee at Semicon Korea 2015

ASML

pSi Membrane is Robust



Regular shipping box



ASML
Wilton

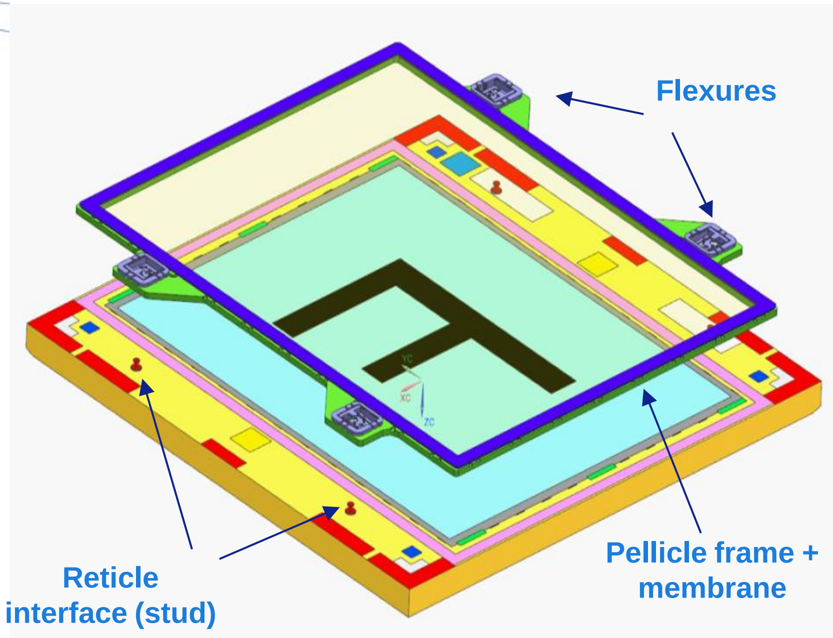
Pelliclized reticle shipped across the US with the film intact.

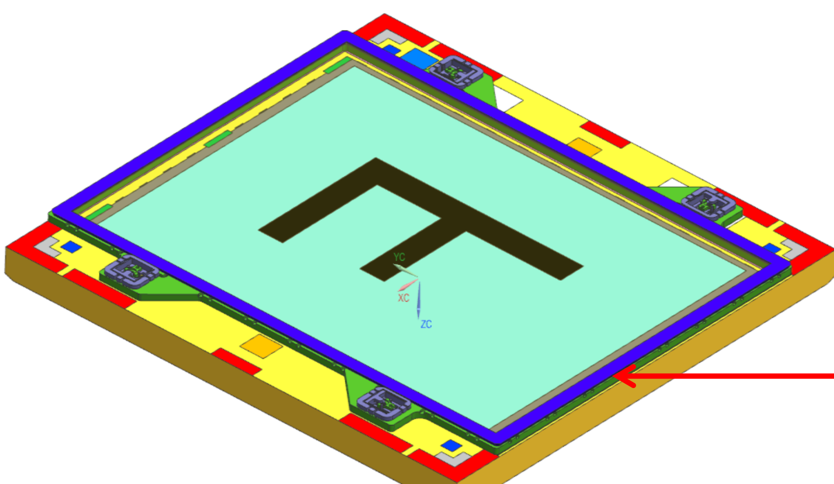
Pictures courtesy ASML, as shown by Sang Lee at Semicon Korea 2015

Interchangeable NXE Pellicle concept

ASML

Allowing multiple inspection schemes





Key features

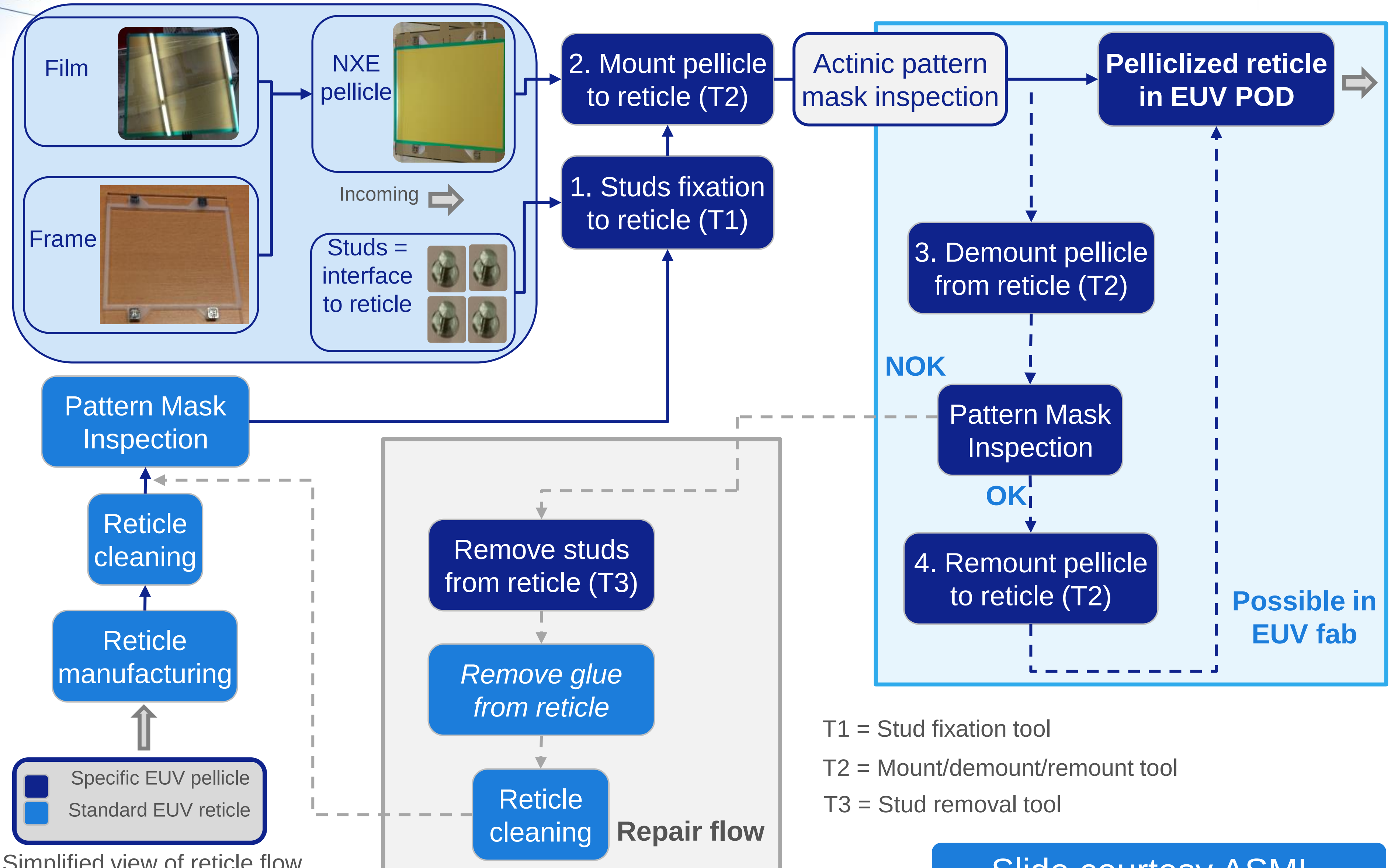
- Reticle front side defect-free solution
  - protects reticle front side from fall-on defects
  - particle free material combination and mounting technology to prevent particle generation
  - additional particle suppression towards pattern area
- Designed for use in NXE scanner
  - pump down/vent cycles compatible
  - vacuum and H_2 environment compatible
  - meets outgassing requirements
  - no overlay impact, distortion-free mounting
- Compatible with standard EUV mask flow
  - concept supports any type of pattern mask inspection: optical, e-beam, and actinic; both at mask shop and fab
  - allows for reticle repel cycle

1. Pellicle frame is not sealed. 200um gap needed for pump-down
2. ASML simulation predicts 1/200 attenuation of small particles
3. Critical to verify!

Slide courtesy ASML.

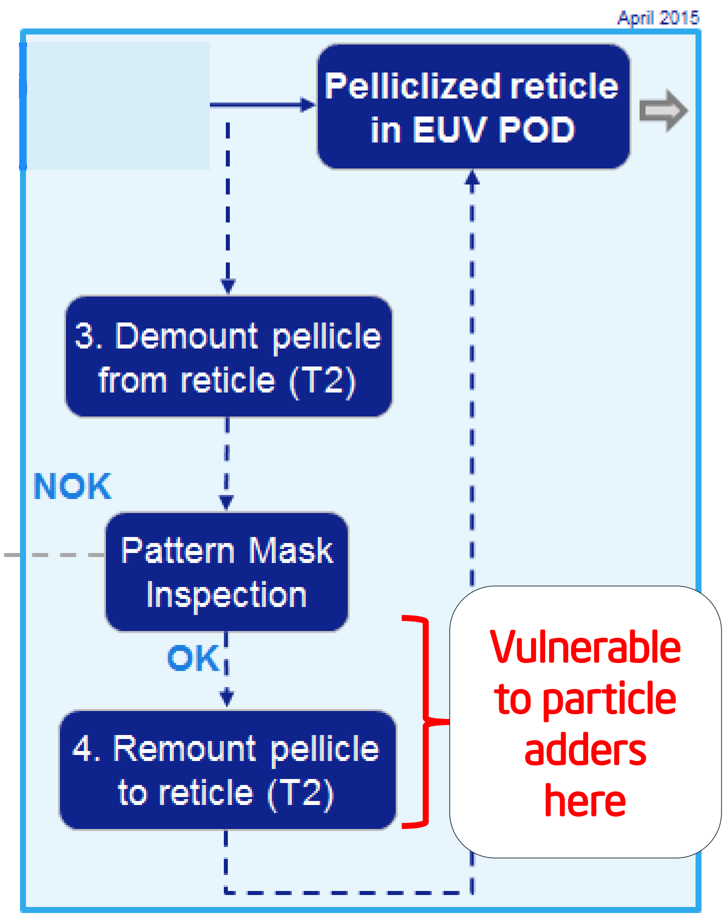
Interchangeable NXE pellicle concept

offers maximum flexibility to EUV mask shop back end and fab reticle flow



Slide courtesy ASML.

Pellicle removal for inspection



- Allows use of existing DUV inspection tools while pellicle is off
- Addresses tracking of PID growth (but at risk of adding particles)
- Could also use e-beam reticle inspection tool, but likely dirty
- Still vulnerable to undetected particles added between inspection and pellicle re-mount
- Any particles added will require removal of posts and reticle clean
- Likely desirable to integrate pellicle remove/replace into inspection tool to minimize time without pellicle protection

Pellicle summary

- Commitment by ASML to commercialize EUV pellicles is good news for EUV end-users
- Removable pellicle design is clever and impressively engineered
- Need to verify particle attenuation by 200um gap
- Does not eliminate need for post-pellicle mount/remount inspection
- Need industry engagement to integrate into mask tools and mask process flow

EUV Infrastructure Readiness Snapshot

EUV infrastructure has 8 key programs

2 are ready or near-ready now, 4 are in development, 2 have significant gaps

- **E-beam Mask Inspection:** HVM capable tool exists
- **Actinic Blank Inspection (ABI):** EIDEC-led tool development program
- **EUV resist QC:** Industry-wide QC center finalizing definition
- **AIMS Mask Inspection:** SEMATECH-led tool development program
- **EUV blank quality:** Process and yield improvements ongoing
- **Pellicle:** ASML commercializing
- **Blank multi-layer deposition tool:** Improving defect results. Multiple deposition techniques being evaluated to define HVM tool approach.
- **Post-pellicle mask inspection:** APMI not on timeline for insertion. Need other options.

EUV reticle inspection roadmap prior to EUV pellicle feasibility

Original industry plan for EUV reticle inspection:

- Extend ArF inspection
- Use e-beam inspection as low-productivity bridge
- Develop Actinic (13.5nm) Patterned Mask Inspection (APMI) tool for sensitivity and productivity

But…

- Neither e-beam nor ArF can inspect through pSi pellicles
- Development of APMI stalled due to high-cost and long lead time (~4 years?)

Proposed alternatives to APMI

- Make EUV scanner so clean a pellicle is not necessary
- Make pellicle mounting perfectly clean **and** hope nothing happens to pattern under pellicle
- Inspect through pellicle with long wavelengths
- Use Patterned Wafer Inspection (PWI) to detect repeating defects
- Accept the cost of yield loss due to repeating defects

Make pellicle mounting perfectly clean and hope nothing happens to pattern under pellicle

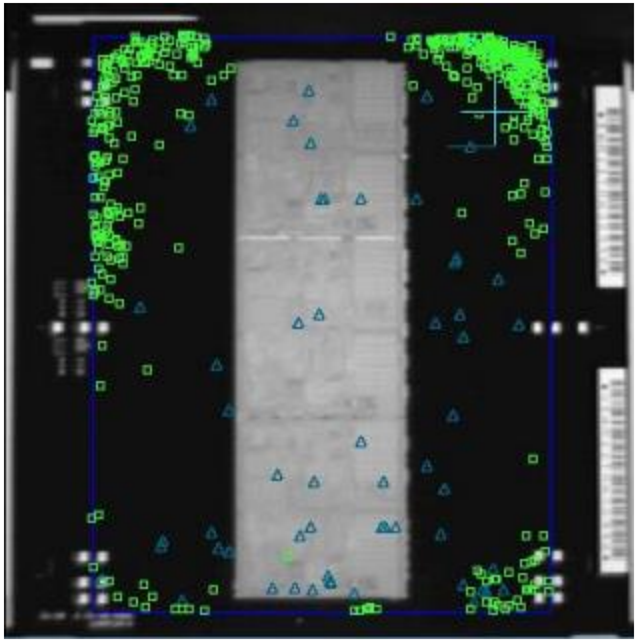
- 365/248/193nm pellicle mounting is not perfectly clean after decades of work by mask shops.

- Various photo-induced defect (PID) mechanisms have plagued 193 masks for >10 years.

- PID mechanisms in vacuum with 13.5nm photons are unknown.

- Area under pellicle will not be purged and will contain outgassing from pellicle frame and adhesives

PID growth on Intel 193 mask



Eschbach *et al.* Proc. of SPIE Vol. 5853

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Use Patterned Wafer Inspection (PWI) to detect repeating defects

Idea:

- Print wafer with reticle under test
- Inspect with patterned-wafer inspection tool
- Filter for defects appearing in more than N fields

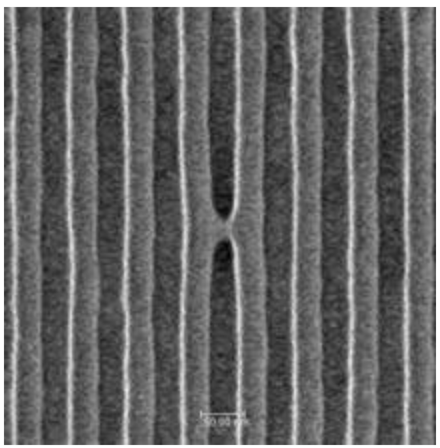
Consider:

- Printing with 13.5nm light
- Inspecting with dry DUV optics at 1X (that is, wafer level)

What do you expect to happen?

Example of limitations of PWI for reticle inspection

- 32/32 L/S reticle with Programmed Defect Array
- Exposed on TW for optimal inspection sensitivity
- Exposed ~ daily to determine capture rate



Example SEM image of programmed defect as printed on wafer

Detection rate

Defects Small ← Large

1	47	47	47	47	47	47		47	47
2	47	47	47	47	47	47		47	47
3	47	47	47	47	46	47		47	47
4	47	47	47	47	46	47		47	47
5	47	47	47	47	47	47		47	47
6	47	47	47	47	47	47		47	47
7	47	47	47	47	46	47		47	47
8	47	47	47	47	46	47		47	47
9	47	47	47	47	46	47		47	47
10	47	47	47	47	46	47		47	47
11	47	47	47	47	47	47		47	47
12	47	47	47	47	45	46		47	47
13	47	47	47	47	46	47		47	47
14	46	47	47	47	46	47		47	47
15	47	47	47	46	45	46		47	47
16	44	44	47	45	41	45		47	47
17	43	44	47	46	41	45		47	47
18	41	43	47	45	38	43		45	47
19	38	44	47	42	36	43		44	47
20	39	44	47	44	37	43		45	47
21	29	36	45	35	25	37		36	46
22	28	25	24	27	21	23		24	33
23			17	11		16			21
24		11	32	10		13		15	31
25									
26									
27									

Run number

Printed and detected in all 47 fields

Printed but detected in no fields

Printability limit

As presented at PMJ, regarding PWI with DUV

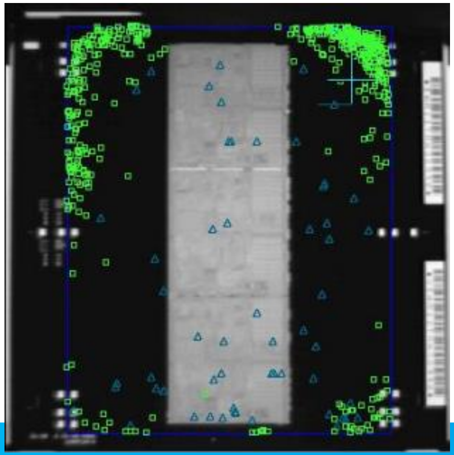
PWI conclusions

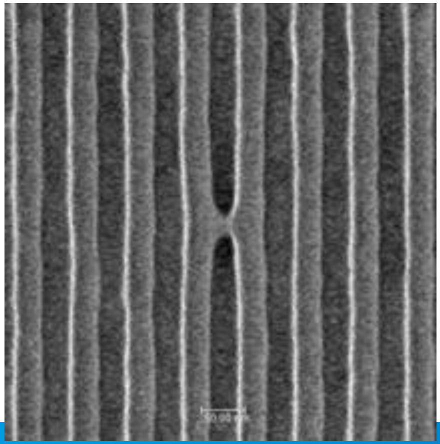
- Misses small defects even on line/space patterns on test wafers, where inspection tool has best sensitivity
- Detection of single missing vias is much more difficult, as is detection on product wafers
- Measured distribution of particles on EUV masks at Intel shows majority of defects will be small (e.g. impact to single via)
- Not useful for tracking PID growth
- Would require much higher resolution inspection than current DUV optical

AMPI vs high-resolution PWI

- Direct inspection of reticle pattern through pellicle is still preferred due to ability to track PIDs or other mask degradation prior to printability
  — But, high cost, low TAM, and long-lead time mean it is unlikely to be available in time for HVM insertion

- Investment in high resolution PWI (e.g. e-beam) benefits in-line wafer inspection in addition to enabling post-pellicle EUV reticle verification



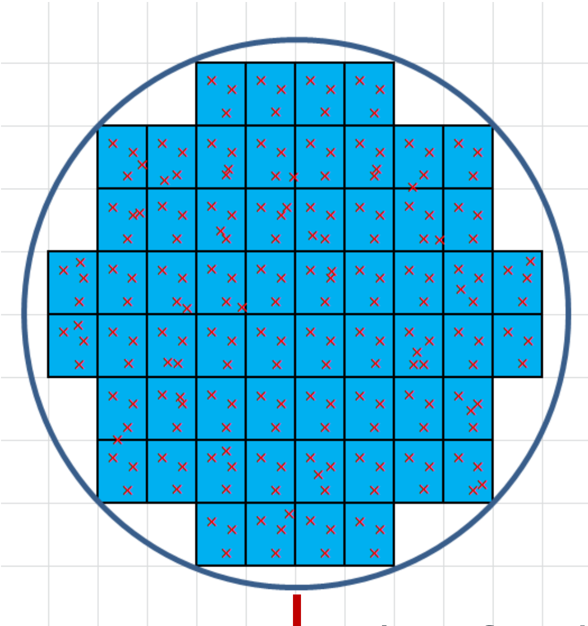


High resolution PWI requirements for post-pellicle reticle verification

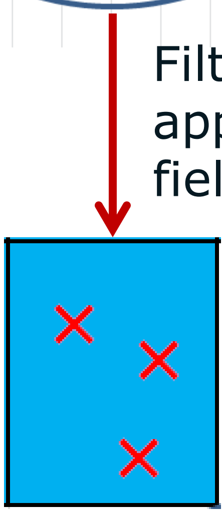
- Need high-sensitivity, high-throughput inspection providing:
  - Sensitivity to 10% delta-CD/CD defects on wafer.
  - Throughput supporting multiple reticle qualifications per day.
  - Low material damage for develop check applications.

High-resolution PWI throughput requirement

DUV inspection



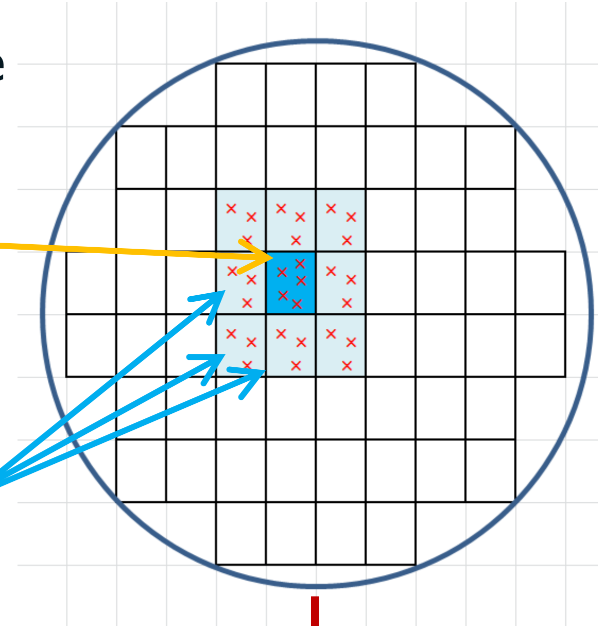
Inspect all fields (poor capture rate)



Filter for defects appearing in >n fields

High-Res inspection

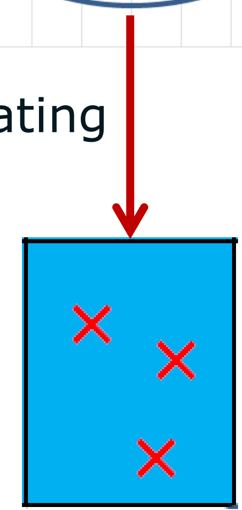
Inspect one full field at high res (~1nm)



Review in a few other fields

Filter for repeating defects

In HVM, need to inspect ~800mm^2 in ~4hrs or less



Conclusions

- Two years of solid progress on source power have debunked claims that EUVL can never achieve high productivity
- Availability, stability and operating cost of source are still concerns
- Infrastructure (mostly mask-related) is in danger of limiting use of EUVL in HVM

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